SIMATIC NET

ASPC 2 / HARDWARE

User Description Date 05/22/97

Order No.

SIEMENS

SIMATIC NET

ASPC 2 / Hardware

User Description

(Advanced PROFIBUS Controller
according to EN 50 170)

Version: V1.0
Date: 05/22/1997

Liability Exclusion
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1 Introduction

1.1 General

Siemens offers its users ASICs for simple high-speed digital data communication between programmable controllers. Designed in accordance with part 1 of PROFIBUS EN 50 170, these ASICs either support or completely handle data communication between the individual programmable controller stations.

The **SPC** (**S**iemens **P**ROFIBUS **C**ontroller) is built directly on layer 1 of the OSI model and requires an additional microprocessor for implementation of layers 2 and 7. This covers all types of protocols on the user side.

The SPC supports active and passive stations on the bus system and filters out all foreign telegrams and incorrect user telegrams.

The parts of layer 2 which execute the bus protocol have already been integrated on the **SPC2**. An additional microprocessor is required for the remaining functions of layer 2 (i.e., interface service and management).

With integration of the complete PROFIBUS-DP protocol, the **SPC3** relieves the processor significantly and can be used on the bus at 12 Mbaud.

The **SPC4** permits the protocol types DP, FMS and PA, and can also be operated on the bus at 12 Mbaud.

The chips support passive stations on the bus system and filter out all foreign telegrams and incorrect user telegrams.

In automation applications, simple devices (e.g., switches, thermo elements and so on) also exist which do not require a microprocessor to acquire their states.

An additional ASIC called the **LSPM2** (i.e., Lean Siemens PROFIBUS Multiplexer)/**SPM2** is available for inexpensive adaptation of these devices. Both ASICs operate as slaves on the bus system. A master addresses the ASICs over layer 2 of the 7-layer model. After a correct telegram has been received, these two ASICs automatically generate the required response telegrams in accordance with part 3 of EN 50 170.

The **ASPC2** communication chip (i.e., Advanced Serial PROFIBUS Controller) handles layers 1 and 2 of PROFIBUS EN 50 170 completely. At the same time, ASPC2 provides a master for PROFIBUS-DP and also PROFIBUS-PA (i.e., Process Automation) using a segment coupler. All ASICs are available on the market and can be ordered from Siemens offices.

1.2 Marketing of ASPC2 Software

The ASPC2 ASIC requires extensive software (i.e., approx. 64 Kbytes) for use as a DP master. Use of the software requires a license. Master license fees are DM 30,000.-- for object code and DM 90,000.-- for source code, regardless of the number desired.

1.3 Software Structure

The following diagram gives a brief overview of the software structure of the master package. For a detailed description, see the **ASPC2 / Software** documentation.

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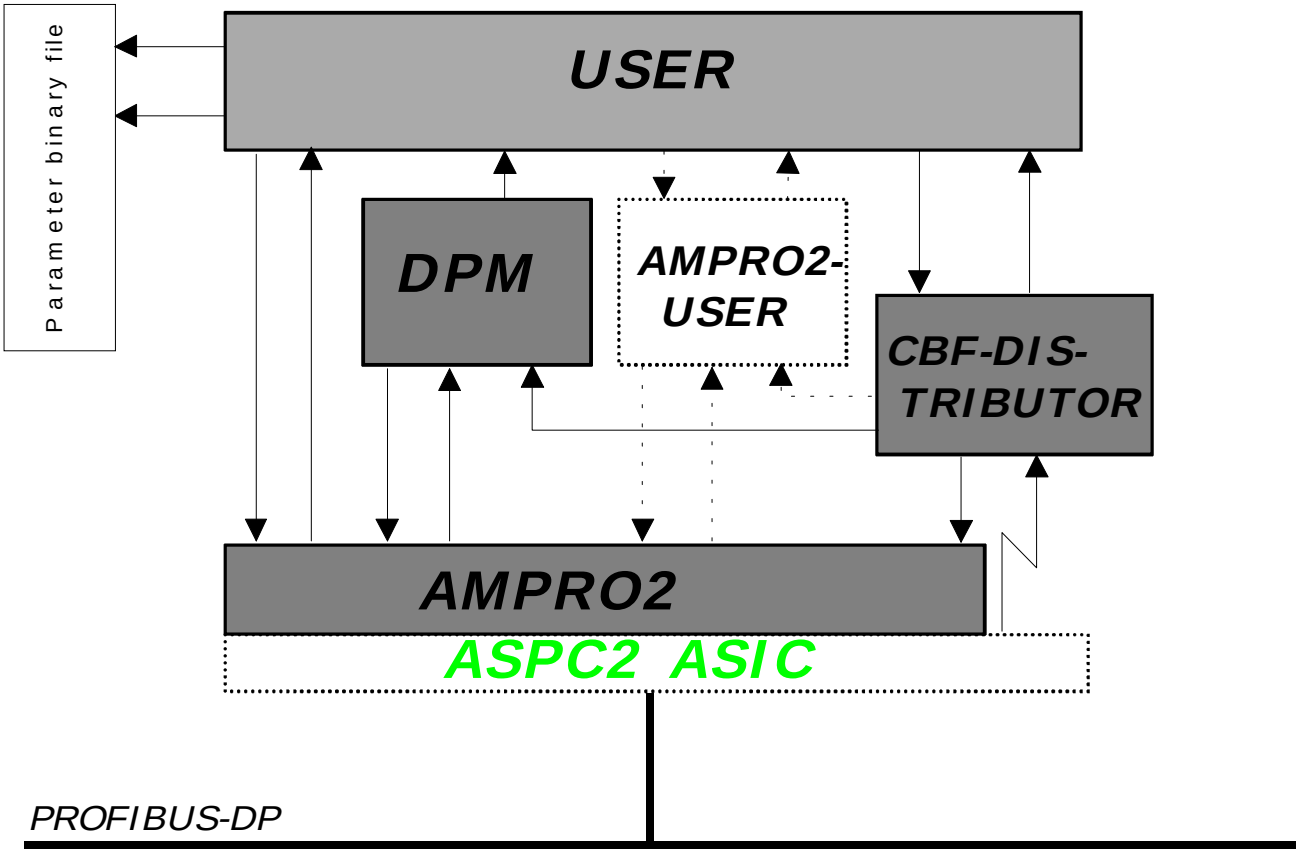

Finished software modules

User program

Function calls

Interrupt

Parameter file created by COM

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2 Function Overview

2.1 Overview of the ASICs

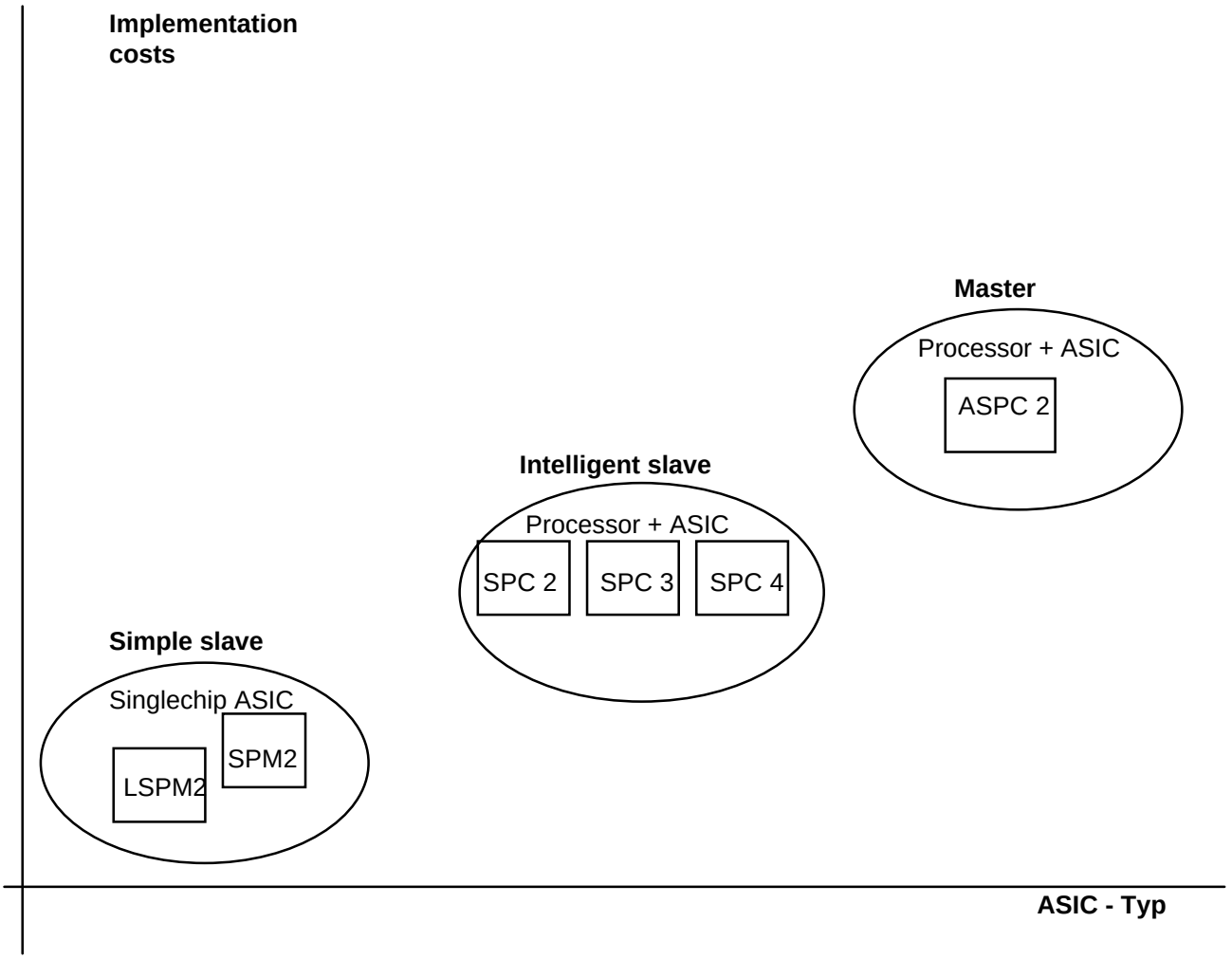

Figure 1: Overview of the ASICs

2.2 Application Areas of ASPC2

ASPC2 is the consistent further development of the ASIC line for PROFIBUS.

The ASPC2 communication chip handles layers 1 and 2 of PROFIBUS EN 50 170 completely. At the same time, ASPC2 provides a master for PROFIBUS-DP and also PROFIBUS-PA using a segment coupler.

This highly integrated controller chip finds use both in manufacturing applications and process engineering.

ASPC2 provides significant relief in the area of communications tasks for programmable controllers, personal computers, drive controllers, process control systems all the way down to operator control and monitoring systems.

The PROFIBUS ASICs are used in slave applications to link lower-level devices (e.g., controllers, actuators, measuring transducers and decentral I/O devices). See Figure 1.

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Special characteristics of the ASPC2 ASIC

- PROFIBUS-DP , PROFIBUS-FMS and PROFIBUS-PA are supported by a single chip.
- High user data throughput
- Support of DP communication for very fast reaction times
- All token management and job processing
- Optimal link to all popular processor types
  No time frame requirements placed on the microprocessor

Interface to the host

- Processor interface
  Can be set to 8/16 bits
  Can be set to Intel/Motorola Byte Ordering
- User interface
  ASPC2 can externally address 1 Mbyte as communication RAM.
- Memory and microprocessor can be linked with the ASIC in shared memory mode or in dual-port memory mode**.**
- In shared memory mode, several ASPC2s can be operated equally on a microprocessor.

Services supported

- Ident
- Request FDL status
- Send Data with No acknowledge (SDN) Broadcast/Multicast
- Send Data with Acknowledge (SDA)
- Send and Request Data with reply (SRD)
- SRD with distribution data base (ISP expansion)
- SM services (ISP expansion)

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Transmission speeds

- 9.6 ; 19.2 ; 93.75 ; 187.5 ; 500 kbit/sec ;
- 1.5 ; 3 ; 6 and 12 Mbit/sec

Reaction times

- Short acknowledgment (e.g., SDA): From 1 msec (11 bit times)
- Typical (e.g., SRD) From 3 msec

Number of stations

- 127 active/passive, mixed as desired
- 64 service access points (SAP) and one default SAP each

Transmission procedure in accordance with

- EN 50 170 PROFIBUS standard, parts 1 and 3
- ISP Specification Draft 3.0 (asynchronous serial interface)

Ambient temperature

- Operating temperature: -40° C to + 85° C
- Storage temperature: -65° C to +150° C
- Chip temperature during operation: -40° C to +125° C

Physical design

- P-MQFP 100 housing 14 x 20 mm^2
  or 17.2 x 23.2 mm^2

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2.3 ASPC2 Step C

Since the current version of ASPC2 is the Step C version, all values and tables are designed for Step C.

Since this ASIC differs only slightly from its predecessor, Step B can be directly replaced with Step C and its advantages when the following points are adhered to.

2.3.1 XWRL-XWRH Mode

This mode is set by circuiting pin 33 and can no longer be parameterized via mode register 1. Its previous function as test output is now on pin 35.

- ☞ Pin 33 is equipped with an integrated pull-up resistor so that when not circuited, XBHE/XWR mode is on after a hardware reset (as with Step B).
- ☞ The pin changes must be considered when test mode is used.
- ☞ The meaning of the bit in mode register 1 has now changed.

2.3.2 Reset Input

This input is a CMOS Schmitt trigger input. The RTS output is deactivated immediately when a reset is performed.

2.3.3 CLK48 Input

This input is a CMOS Schmitt trigger input. Distortion of the pulse duty factor has been eliminated and can now be 80/20 or 20/80.

2.3.4 Bus Access

The ASIC has a faster data transfer cycle time and, with a setting in mode register 2, can be operated in quick access mode which further shortens cycle times.

2.3.5 Guaranteed Operating Range

Temperature range: -40 C to +85 C
DC supply voltage: +5 V, ± 10%

2.3.6 Release Status

The release status can be read from address 0BH.

- ☞ Step B (value = 0) or Step C (value = 1)

2.3.7 Lock Handling

Lock handling of ASPC2 can be set by the user in dual-port memory mode.

2.3.8 EOI Inactive Time

The time between EOI and the next possible interrupt can be parameterized to 1 µsec or 1 msec. Monitor mode has a different time base.

2.3.9 User Timer Interrupt

Using the delay timer, the user can implement a software timer (except in ISP and monitor mode) which can be set with mode register 2 to 2.1 sec or 10 msec.

2.3.10 Blocked Mode

This setting can be used to hold back input data which are shorter than the FIFO until the entire telegram has been received and checked for correctness. This function is no longer dependent on the DP mode setting. It is now dependent on a setting in mode register 2 instead.

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2.3.11 FIFO Size

As with Step B, the size of the FIFO can be set to 64 or 128 bytes in mode register 2.

2.3.12 Time Between Two Tokens

In pass token status, a wait time of Tid1 is maintained between two consecutive token telegrams.

2.3.13 XCTS Control

In monitor mode, recording is only performed when the XCTS input contains a logical 0. Otherwise the telegrams are filtered.

2.3.14 Data Pointer Exchange

The data pointers can now also be exchanged on the master when a repeat is being executed.

2.3.15 NOP Job

Jobs with this option are no longer sent.
Example: FORCE-PASS-TOKEN job

2.3.16 Data Length for Repeat

When the repeat job has a response length of zero, the check with the set expected length is omitted.

2.3.17 Consistency Signals for the Slave

The consistency signals WRCONS and RDCONS can now also be generated for use with slaves.

2.3.18 IND-APB in Repeat Mode

By setting a flag in the application block, it is now possible to remove the block from the SAP list even when the repeat condition is fulfilled.

2.3.19 Clear Mode Setting

A setting in the request blocks can be used to determine which data will be sent to the slaves in CLEAR mode (mode register 1).

- ☞ Data bytes can all be set to zero.
- ☞ Data length can be set to zero.

2.3.20 Data Length

When the data lengths of L2 and L4 are greater than 250D, the job is directly confirmed with 8EH without sending a telegram.
When the length of the data received by the slave is less than the specified L4 data length, an RS is now given in response.

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2.4 ASPC2 Step D

Starting around March of 1997, the Step D version of ASPC2 will be available.
The Step C version of ASPC2 can be directly replaced with Step D provided the following points are adhered to.

2.4.1 Release Status

The release status can be read from address 0BH.
☞ Step C (value = 1) or Step D (value = 2)

2.4.2 GAP Error in DP Mode

The error that caused a wrong GAP area to be processed in DP mode under certain circumstances has been corrected in Step D.

2.4.3 Return Error for Repeat Indication Resources

The error which sometimes caused the indication resources to be returned although the repeat specification was fulfilled has been corrected in Step D.

2.4.4 Deadlock Error for Incorrect Hardware Circuitry

When an incorrect hardware circuit prevented ASPC2 from accessing the request data block with a ready-delay (approx. 15 µsec at 12 Mbaud), this could still cause a deadlock with Step C. This deadlock has now been corrected in Step D.

2.4.5 Fail-Safe Mode for ASPC2 as Slave

Fail-safe mode can be activated for repeat blocks in a SAP with a setting in the 'fc' field of the indication application block.

2.4.6 RTS Advance

By entering a value in the 'MON selector 1' register, the setup time of the RTS signal can be set for the TxD signal. When the Step D ASPC2 is reset, the value 1 is used for reasons of compatibility.

2.4.7 SC Filter in Monitor Mode

When the setting 'SD4 filter = 1' is used, Step D also filters the short confirmations (SC) of the filtered request telegrams.

2.4.8 Change in Response Status for ASPC2 as Slave

By making a setting in the 'resp-status' field of the reply-update application block, it can be specified whether ASPC2 is to automatically change the priority of the response telegram from high to low after the telegram has been sent.

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3 Pin Description

ASPC2 is equipped with a 100-pin P-MQFP housing.

01: XRD	T	26: XREQ	T	51: AB11		76: DIA5	
02: DT/XR		27: XREQRDY		52: AB10		77: VSS	
03: VSS2		28: XENBUF		53: VSS		78: DIA4	
04: VDD3		29: VSS2		54: VDD3		79: DIA3	
05: XBHE/XWRH	TPU	30: XINT/MOT	CPD	55: AB9		80: VSS2	
06: HOLD		31: XTEST0	C	56: AB8		81: DIA2	
07: DB7	TPU	32: XTEST1	C	57: AB7		82: DIA1	
08: DB6	TPU	33: XWRL_MODE	CPU	58: AB6		83: DIA0	
09: VDD		34: XCTS	C	59: VDD		84: X/INT-EV	
10: VSS		35: DIA9		60: VSS		85: X/INT-CI	
11: DB5	TPU	36: XB8/B16	CPU	61: AB5	T	86: RTS	
12: DB4	TPU	37: XWR/XWRL	T	62: AB4	T	87: TXD	
13: DB3	TPU	38: AB19		63: AB3	T	88: DB15	TPU
14: DB2	TPU	39: AB18		64: AB2	T	89: DB14	TPU
15: VDD		40: VDD		65: VDD		90: VDD	
16: VSS		41: VSS		66: VSS		91: VSS	
17: VSS3		42: AB17		67: VSS3		92: VSS3	
18: DB1	TPU	43: AB16		68: AB1	T	93: DB13	TPU
19: DB0	TPU	44: AB15		69: AB0	T	94: DB12	TPU
20: X/HOLDAOUT		45: AB14		70: XCLK2		95: DB11	TPU
21: X/HOLDAIN	T	46: VSS		71: CLK	CS	96: DB10	TPU
22: RESET	CS	47: VDD		72: XHTOK		97: VSS	
23: RXD	C	48: VSS2		73: DIA8		98: VDD	
24: XRDY	T	49: AB13		74: DIA7		99: DB9	TPU
25: XCS	T	50: AB12		75: DIA6		100: DB8	TPU

Table 1: Pin allocation

VDD: Output pads and internal locations
VDD3: Input pads
VSS: Output pads
VSS2: Internal locations
VSS3: Input pads
T: TTL level
TPU: TTL level with pull-up
C: CMOS input
CPU: CMOS input with pull-up
CPD: CMOS input with pull-down
CS: CMOS-Schmitt-Trigger input

3.1 Description of the Inputs

Signal Name	Quantity	Function	Source
CLK	1	Clock pulse input (48 MHz)	System support
RESET	1	Hardware RESET	CPU, port
XCS	1	Chip Select	System support
XRDY	1	Asynchronous READY	System support
X/HOLDAIN	1	Hold-Acknowledge- In	CPU or existing ASPC2
XREQ	1	Bus request from ext. master	System support
RXD	1	Serial receiving channel	RS 485 receiver
XCTS	1	Clear to Send	FSK modem

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XB8/B16	1	System bus configuration	Soldered jumper
XINT/MOT	1	System bus configuration	Soldered jumper
XWRL-Mode	1	80C165 interface: XWRH, XWRL	Soldered jumper

Table 2: The 11 Input pins of ASPC2 (without test inputs)

3.1.1 Test Pins

During normal operation, the two test pins XTEST0 and XTEST1 must be applied to VDD with a resistor (+5 V).

3.2 Description of the Outputs

Signal Name	Quantity	Function	Destination
X/INT-CI	1	Interrupt confirmation/indication	CPU or IR controller
X/INT- EVENT	1	Interrupt event register	CPU or IR controller
DT/XR	1	Data Transmit Receive	System support
HOLD	1	HOLD request	CPU
X/HOLDAOUT	1	HOLD-ACK-OUT	Next ASPC2
XENBUF	1	Enable ext. buffer on X/REQ	System support
XREQRDY	1	Ready for ext. bus master	CPU or system support
TXD	1	Serial sending channel	RS 485 sender
RTS	1	Request to send	RS 485 sender
AB19 .. 6	14	Address bus	Memory, system support
DIA9.. 0	10	Diagnosis port	System support
XHTOK	1	Hold token indication	LED
XCLK2	1	24 MHz clock	System support

Table 3: The 35 output pins of ASPC2

3.2.1 Diagnosis Port

By parameterizing the variable DEBUG-MODE1..0 in mode register 0, either the address bus of the micro-sequencer, the address bus of the channel sequencer, the monitoring signal ‘BUSLOCKOUT’ or the checking signals ‘RDCONS’ and ‘WRCONS’ can be applied to this port for support of consistency control.

DEBUG-MODE1..0	DIA9	DIA8-2	DIA1	DIA0
0 0	MSADR(9)	MSADR(8-2)	WRKONS	RDKONS
0 1	MSADR(9)	MSADR(8-2)	MSADR(1)	MSADR(0)
1 0	BUSLOCKOUT	KSADR(8-2)	WRKONS	RDKONS
1 1	BUSLOCKOUT	KSADR(8-2)	KSADR(1)	KSADR(0)

3.3 Bi-Directional Signals

Signal Name	Quantity	Function	Source/Destination
AB5 .. 0	6	Address bus	CPU, memory, system support
DB15.. 0	16	Data bus	CPU, memory
XBHE	1	Byte high enable	CPU, memory
XRD	1	Read	CPU, memory
XWR	1	Write	CPU, memory

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Table 4: The 25 bi-directional pins of ASPC2

Other signals:	VDD pins	10
	VSS pins	17
	Test pins	2

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4 ASIC Interface

4.1 Address Window

ASPC2 must be addressed by the processor in so-called I/O mode for parameterization and interrupt event handling. A small address area of 64 bytes is available for this purpose. An ASPC2 register is not selected unless the 'XCS signal' and the appropriate offset address are set up.

Read		Write		OFF-ADR
High(A0=1,XBHE=0) High(A0=0,XBHE=1)	Low(A0=0.XBHE=1) Low(A0=1,XBHE=0)	High(A0=1,XBHE=0) High(A0=0,XBHE=1)	Low(A0=0.XBHE=1) Low(A0=1,XBHE=0)	Intel Motorola
TTHOLD15..8	TTHOLD7..0	TTR15..8	TTR7..0	00H
Delay-Timer 15..8	Delay-Timer 7..0	INT-MASK-REG15..8	INT-MASK-REG7..0	02H
INT-REQ-REG15..8	INT-REQ-REG7..0	INT-REQ-REG15..8	INT-REQ-REG7..0	04H
INT-REG15..8	INT-REG7..0	INT-ACK-REG15..8	INT-ACK-REG7..0	06H
Status-REG15..8	Status-REG7..0	Mode-REG015..8	Mode-REG07..0	08H
Status-REG31..24	Status-REG23..16	Mode-REG1-Set15..8	Mode-REG1-Set7..0	0AH
-	LAS-REG3..0	Mode-REG1-Res15..8	Mode-REG1-Res7..0	0CH
		SCB-BASE-LW15..8	SCB-BASE-LW7..0	0EH
		SCB-BASE-HW31..24	SCB-BASE-HW23..16	10H
		TSLOT-REG13..8	TSLOT-REG7..0	12H
		TID1-REG9..8	TID1-REG7..0	14H
		TID2-REG9..8	TID2-REG7..0	16H
		TRDY-REG9..8	TRDY-REG7..0	18H
		BR-REG10..8	BR-REG7..0	1AH
		SAP-MAX7..0	TS-ADR-REG70	1CH
		Token-Err-Limit7..0	GUD-REG7..0	1EH
		TQUI-REG7..0	LAY4-HLen-REG7..0	20H
		Resp-Err-Limit3..0	HSA 6..0	22H
		MON-Selektor2 7..0	MON-Selektor1 7..0	24H
		Mode-REG25..0	Retry-Tok 3..0 / Retry-Msg 3..0	26H
		WAIT-STATES15..8	WAIT-STATES7..0	28H

Table 5: Internal ASPC2 registers

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Token rotation timer (register):
Register for parameterization of the desired token rotation time (T_{TR}). The token hold time (T_{THOLD}) can be read for system initialization.

Interrupt controller register:
Register for handling and evaluation of the interrupts

Status register:
Register with the current status of ASPC2

LAS register:
This register can be used by the processor to read the LAS RAM. Each access increments the internally generated LAS RAM address.

Mode register:
Mode registers 0, 1 and 2 are used for parameterization of ASPC2.

The following hardware settings can be made.

- Set interrupt outputs via INT-EV or INT-EV, INT-CI
- Set interrupt outputs low or high-active
- Set X/HOLDA signal low or high-active
- Set whether the consistency signals are to be applied to the diagnostic ports
- Set whether shared memory or dual-port memory mode is desired
- Enable or disable quick access mode
- Parameterize active interrupt time
- Activate block mode for amounts of data less than the size of the FIFO
- Number of wait states or ready activation can be set for each of the four 256-Kbyte segments.

SCB-BASE-HW/LW:
Register with the 20/32-bit base address of the system control block

Slot timer register:
Wait for receipt time T_{SL}

T_{ID1} timer register:
Register with the T_{ID1} time (valid after acknowledgment, response or token telegrams)

T_{ID2} timer register:
Register with the T_{ID2} time (valid after a call telegram which is not acknowledged)

T_{RDY} timer register:
Register with the T_{RDY} time (ready time, valid before a response telegram is sent)

Baud rate register:
Register with the scaling factor for the baud rate

TS address register:
Register with the station address

GUD register:
Register with the GAP update time T_{GUD}

Token error limit register:
Parameterization of the number of implausible token telegrams per 256 token rotations before ASPC2 assumes *listen token status*.

SAP MAX register:
Parameterization of the highest SAP list no. generated in SCB

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LAY4 HLen register:
Parameterization of two different layer-4 header lengths

TQUI register:
Parameterization of modulator conclusion time T_{QUI}. In addition, the delay time between XENBUF and XREQRDY can be set here.

HSA register:
Parameterization of the highest active address

Response error limit register:
Parameterization of the number of faulty response telegrams after which double token is assumed

Monitor selector register:
Two address selector registers are available in monitor mode.

Wait states register:
The wait states are parameterized for each 256-Kbyte segment of memory.

Retry register:
The number of telegram and token retries is parameterized here.

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4.2 System Control Block

The system control block (SCB) is used as the interface between ASPC2 and the FLC.
Each job is entered in an application block (REQ-APB) and inserted in the SCB at the appropriate location.
Although ASPC2 can directly address a 1-Mbyte memory area, the SCB and the application blocks must be located in any 64-kbyte segment while the data blocks can be distributed over the 1-Mbyte area.

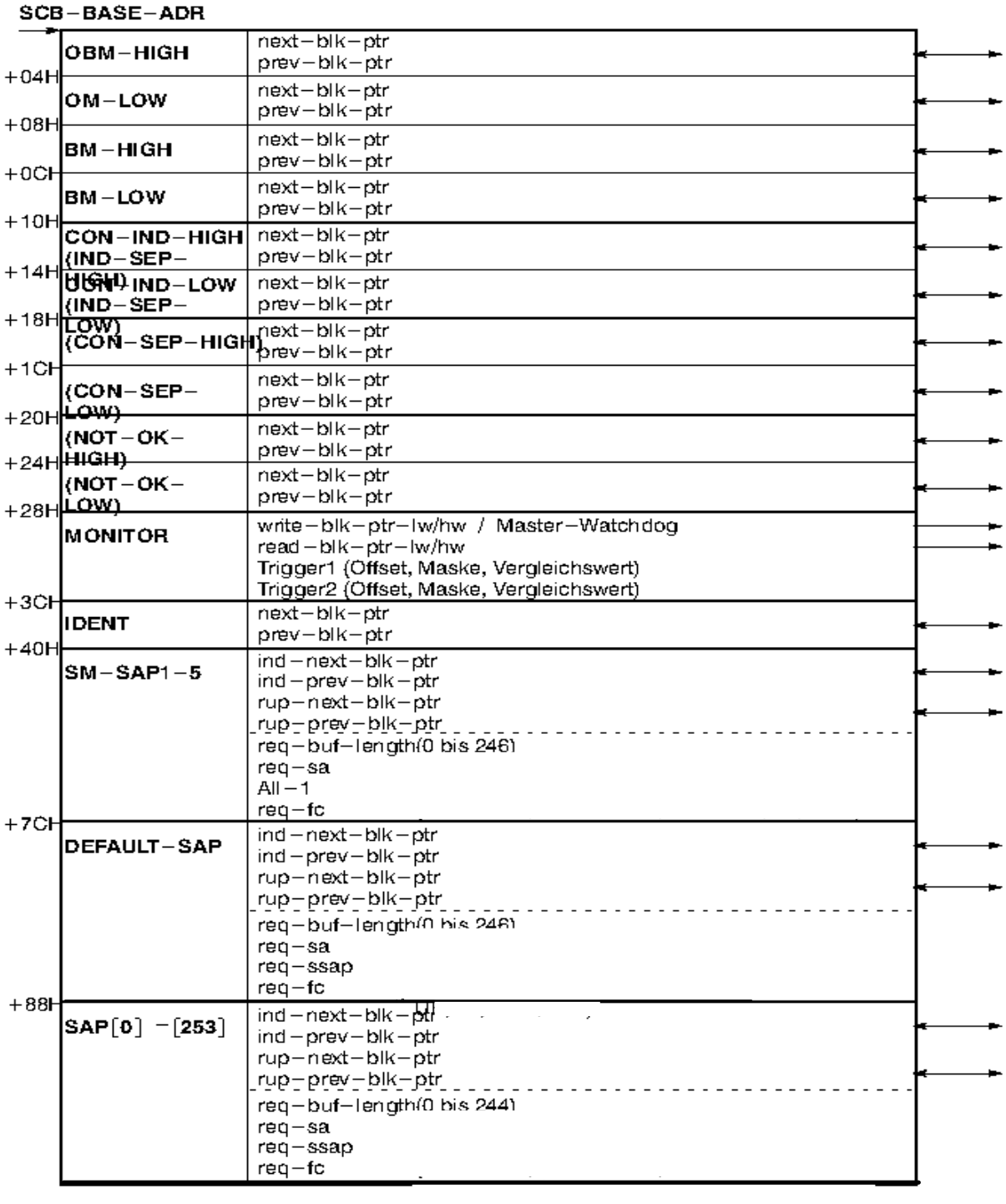

Figure 2: System control block of ASPC2

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4.3 Interrupt Controller

The interrupt controller reports various events to the processor. These events are primarily confirmation/indication messages and various error events. The interrupt controller contains a total of up to 16 events which are connected to one or two interrupt outputs. The controller is not equipped with prioritization and does not supply an interrupt vector.
The controller contains an interrupt request register (IRR), an interrupt mask register (IMR), an interrupt register and an interrupt acknowledge register (IAR).

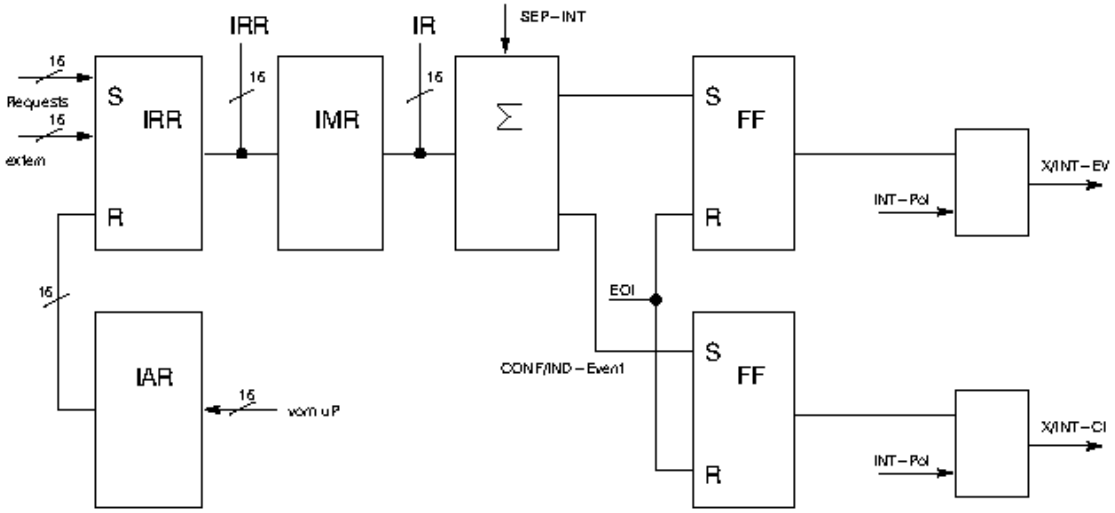

Figure 3: Interrupt controller in ASPC2

Every event is stored in the IRR. The IMR can be used to suppress individual events. Entry in the IRR is not dependent on the interrupt mask. The event signals which are not masked out in the IMR generate the **X/INT-EV interrupt** via an S network. In addition, a second interrupt output is available. Using the "SEP-INT" parameter in mode register 0, the COND/IND can either be circuited to the common X/INT-EV interrupt ("SEP-INT = 0") or to the separate **X/INT-CI interrupt** ("SEP-INT = 1").
When the X/INT-EV is involved, the processor must read the interrupt register (IR) of ASPC2 to determine which interrupt request is involved. The interrupt register is the output of the IMR.

Every interrupt event which has been processed by the processor must be deleted via the IAR (the CON/IND also). This requires that a logical 1 be written in the appropriate bit position. If a new event is available on the IRR at the same time and an acknowledgment of the previous event is waiting, the event remains stored. When the processor subsequently enables a mask, it must be ensured that the IRR does not contain an entry from the past. To be on the safe side, the position in the IRR must be deleted before the mask is enabled.
Before exiting the interrupt routine, the processor must set **"End of Interrupt-Signal (EOI) = 1"** in mode register 1. This change in edge deactivates both interrupt lines. If an event is still stored, that particular interrupt output becomes active again after being deactivated by an EOI. This makes it possible to reenter the interrupt routine by using an edge-triggered interrupt input.
The EOI inactive time can be parameterized from 1 µsec to 1 msec.
The polarity of the interrupt outputs can be parameterized. After the hardware reset, the outputs are low-active.

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5 Processor Interface

5.1 Bus Access

5.1.1 Intel/Motorola

ASPC2 is equipped with an adjustable 8/16-bit bus interface. Setting is performed with pin XB8/B16 (i.e., XB8/ B16 = 0 ! 8 bit bus interface; XB8/B16 = 1 ! 16 bit bus interface). The input is equipped with an internal pull-up resistor. When not circuited, the 16-bit bus interface is used.
Using pin XINT/MOT, it can be operated in both Intel bus format and Motorola bus format. The input is equipped with an internal pull-down resistor. When not circuited, the Intel bus format is used. In 8-bit Intel mode, only the lower data bus byte is connected (i.e., DB7..0). The higher data bus byte is permanently circuited to input and is equipped with internal pull-up resistors. Pin XBHE is also set to input and must not be circuited since it is terminated with an internal pull-up resistor.

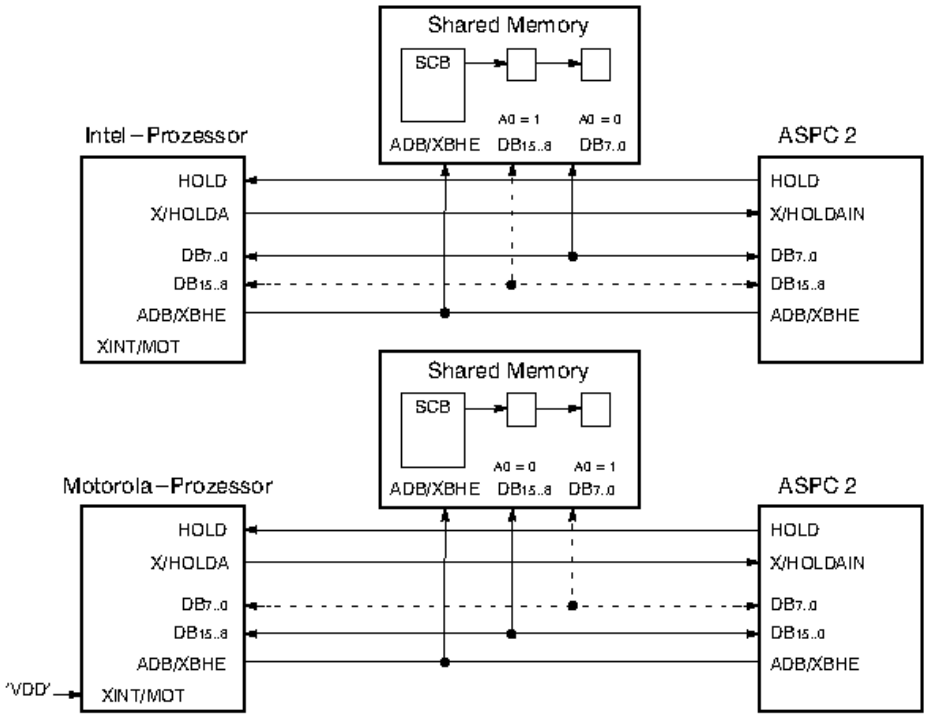

Figure. 4: Connection of the Intel/Motorola processor

When Motorola processors are used, XINT/MOT must be applied to 'VDD'. ASPC2 must be connected in 16-bit mode as in Intel mode. The XBHE signal must be generated externally from the Motorola control signals. The following convention must be adhered to. In 8-bit Motorola mode, only the higher data bus byte is used (i.e., DB15..7). The lower data bus byte is permanently circuited to input and is equipped with internal pull-up resistors. Pin XBHE is also set to input and must not be circuited.
In Motorola mode, all byte positions within a word must be reversed for processor accesses to ASPC2. The same applies to the setup of the SCB and the application blocks. This does not apply to the layer-4 data in the application block and the relocated request and response data blocks. These data areas are set up as byte arrays by the FLC. When these areas are accessed (i.e., DATACCESS=1), ASPC2 reverses the higher byte with the lower byte of an aligned data word.
Caution: The long-word address pointers (e.g., resp-buf-ptr-lw/hw) must be stored by the FLC in word-reversed format in the application blocks.

All ASPC2 accesses to external memory are word-accesses. In 8-bit mode, these word accesses are distributed over two consecutive byte-accesses.

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5.1.2 XWRL/XWRH Mode

To save on external hardware for 80C165 applications, pins XWR and XBHE can be reparameterized to XWRL and XWRH (i.e., XWRL/XWRH mode). The switchover is performed via XWRL mode. This input is equipped with an integrated pull-up resistor. When not circuited, XBHE/XWR mode is used. This ensures compatibility with predecessor equipment.

5.2 Access Times

The bus interface unit (i.e., BIU) operates at half the system clock pulse rate (i.e., 24 MHz at a system clock pulse of 48 MHz) either synchronously with the capability of inserting 1 to 5 wait states via an internal wait state generator, or asynchronously by using additional synchronization of an external ready signal (i.e., XRDY). The wait states can be set separately for each 256-kbyte memory segment.

5.2.1 Simple Access

When 1 wait state is parameterized, the external RAMs of ASPC2/Step C require an access time of 70 nsec. At this setting, read/write access of one data word requires 167 nsec.

5.2.2 Quick Access

With Step C, a quick bus mode is implemented called "Quick Access Mode." In this mode, all external read/write operations are accelerated by a 24 MHz clock pulse. This can only be achieved by compressing the bus timing, however. During read operations, the DT/XR signal has the same phase relation as the XRD signal. This produces a bus cycle time of 125 nsec for the data transmission. With this setting, the external ASPC2 RAMs require an access time of 50 nsec. With this access time, the external RAMs must always be selected. Otherwise even faster RAMs must be used. Each additional wait state increases this time by 41.6 nsec.

5.2.3 Ready Access

When parameterized, access can be performed asynchronously via an external read signal (i.e., XRDY). See Figure 13: Ext. ready timing. 0 or 1 wait states can still be inserted after the ready signal. See Figure 14: Ext. ready timing with wait state after ready.

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5.3 Bus Types

5.3.1 Shared Memory

When the parameterization "XSHMEM/DPMEM = 0" is used, communication between the FLC (processor) and ASPC2 takes place in a shared memory in which the SCB and all lists are stored. ASPC2 accesses this memory in master mode. This requires that the SYS bus be "taken." The HOLD-X/HOLDA signals are used for this handshake. The polarity of X/HOLDA can be parameterized in mode register 0. After the hardware reset, the signal is low-active. ASPC2 uses "HOLD=active" to request the SYS bus and waits until the processor gives it bus access with "X/HOLDA=active." ASPC2 then switches its SYS bus drivers from tri-state to active and begins the memory accesses. **This hold phase cannot be interrupted externally.** When ASPC2 is finished, it switches the drivers back to tri-state and sets "HOLD=inactive." The processor takes control again and acknowledges with "X/HOLDA=inactive."
Several ASPC2s can be daisy chained on one SYS bus. The X/HOLDAOUT signal is available as an additional output via which the next ASPC2 always receives bus access when X/HOLDA is output by the processor and ASPC2s before it have not made bus requests themselves. Priority within the chain is fixed (i.e., the first ASPC2 has the highest priority, and the last ASPC2 has the lowest priority). All HOLD outputs must be circuited together with a wired or-line and terminated with a pull-down resistor.

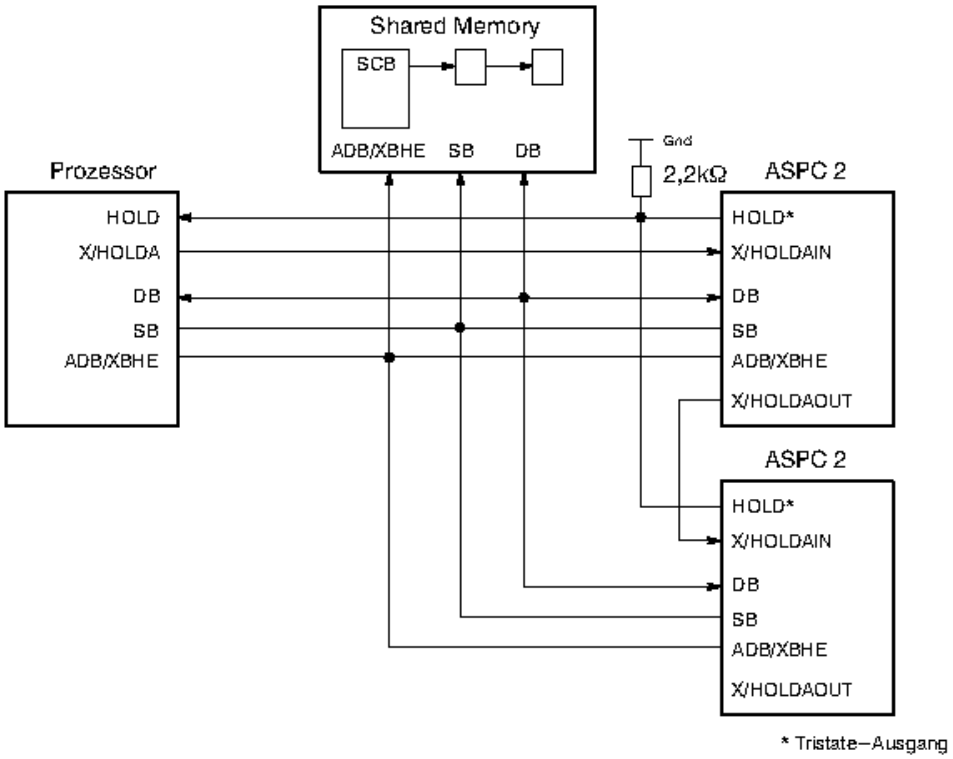

Figure 5: Shared memory

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5.3.2 Dual-Port Memory

In hardware configurations whose processors do not have hold functions or whose applications do not request processor time, this shared memory must be designed as dual-port memory. "XSHMEM/DPMEM = 1" must be parameterized for this purpose in mode register 0. In support, ASPC2 offers an integrated bus arbiter via which an external bus master (i.e., processor) receives access to the SYS bus. An external bus request must be made on ASPC2 for every processor access to ASPC2 or the dual-port memory. The XREQ pin must be active-low. When bus access is granted, ASPC2 first switches the XENBUF output active via which the external data and address bus drivers are switched through to the SYS bus. ASPC2 then switches the XREQRDY output active via which the external signal bus driver (i.e., read or write signal) is enabled and the XRDY signal is sent to the processor. The time between XENBUF active and XREQRDY active can be parameterized with "QREQRDY" (TQUI register) to either 1 clock pulse cycle (T48) or 3 clock pulse cycles (T48).
Several ASPC2 chips cannot be cascaded in this mode.

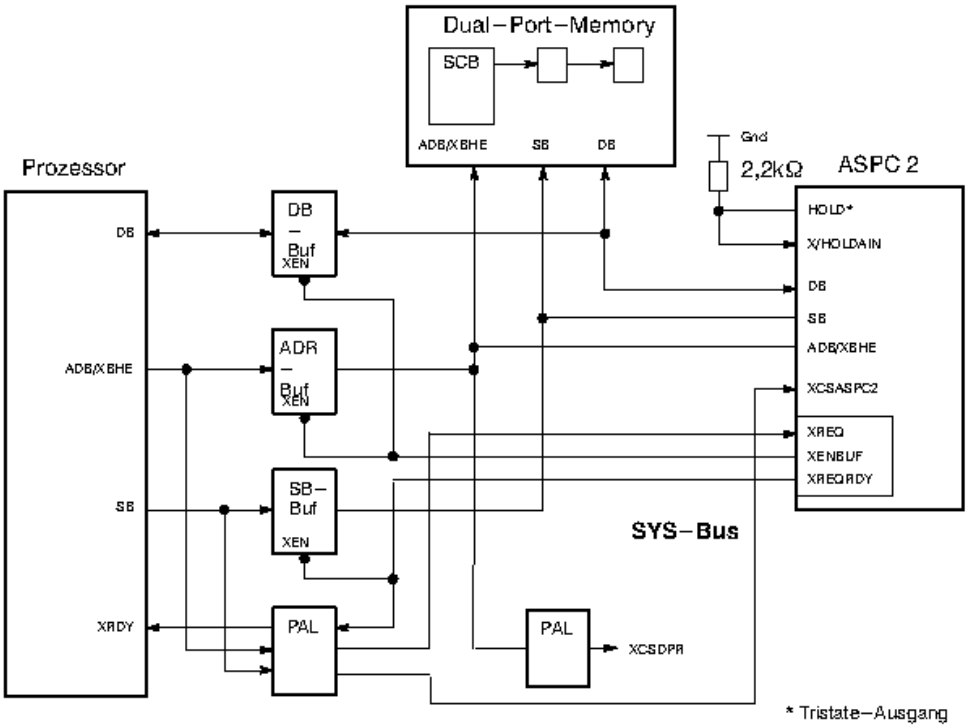

Figure 6: Dual-port memory

5.4 I/O Mode

The processor must address ASPC2 in I/O mode for parameterization and interrupt event handling. Various internal registers can be read or written in a small 64-byte address window. For address assignment, see Table 5: Internal ASPC2 . Access can be performed by word or byte (Intel/Motorola format: controlled via bus signals XBHE and AB0).

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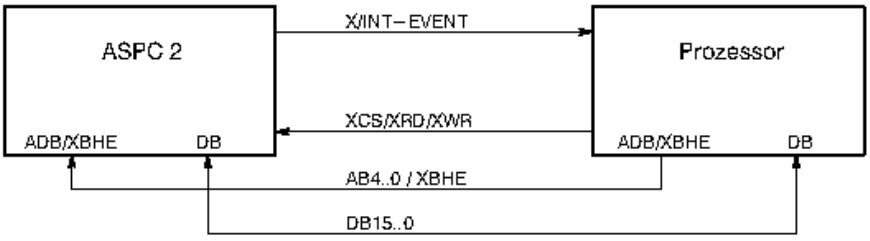

Figure 7: I/O mode

5.5 Data Consistency

Depending on the size of the FIFO, ASPC2 can support a layer-2 data consistency up to 122 bytes. During sending, it fetches the user data using a lock cycle in the internal FIFO. The sending procedure does not begin until ASPC2 has received access to the layer-2 data.
During receiving, the ASIC holds back the user data until the entire telegram has been received correctly. All data are then transferred to the external memory using a lock cycle. When data packets are larger than the specified consistency length, it transfers the user data as soon as the FIFO size is exceeded.
It provides two 'RDCONS/WRCONS' outputs in support of external consistency control logic so that consistent data can be directly transferred by ASPC2 to/from an external image memory. These signals are activated by ASPC2 when layer-2 data are fetched from the memory (RDCONS) or written to the memory (WRCONS). These signals are activated on both the slave and the master. The control signals are enabled in the function code field of the APB so that the user can mix consistent and non-consistent APBs.

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6 Serial Bus Interface

6.1 ASPC2 Signals

ASPC2 is connected with the galvanically isolated interface drivers via the following signals.

Signal Name	Input/ Output	Function
RTS	Output	Request to Send
TXD	Output	Sending data
RXD	Input	Receiving data

6.2 Baud Rate Generator

Baud rates from 9.6 kBd to 12 MBaud can be generated with the baud rate generator (10-bit scaler). A clock pulse of 48 MHz is used. The baud rate generator (i.e., BRG) supplies the receiver with the quadruple transmission clock pulse and the transmitter with the simple clock pulse.

6.3 Transmitter

The transmitter converts the parallel data structure into a serial data flow. The asynchronous UART procedure uses a start bit and a stop bit which enclose the 9 information bits (i.e., 8 data bits and 1 even parity bit). The start bit is always logical 0, and the stop bit and the idle state are always logical 1. The less significant data bit is sent first.
The transmitter contains a transmit buffer and a shift register. The telegram characters are written to the transmit buffer by the MS. This buffer ensures sending without gaps. The sender generates transmit-buffer-empty and transmitter-empty as status signals. Transmitter-empty means that both the transmit buffer and the shift register are empty. The transmitter generates this signal after the stop bit on the SER bus was sent (i.e., sending has been concluded).
Before the MS writes the first telegram character in the transmit buffer, it generates a Request-To-Send (i.e., RTS). The XCTS input can be used to connect a modem. After RTS active, the transmitter must hold back the first telegram character until the modem has activated XCTS. The transmitter does not scan the XCTS again during telegram transmission. When sending has been concluded (i.e., transmitter-empty), the MS withdraws the RTS again.

6.4 Receiver

The receiver converts the serial data flow into the parallel data structure. It scans the serial data flow with four times the transmission rate. Synchronization of the receiver always starts with the negative edge of the start bit. The start bit and the other bits are scanned once in the bit middle (time-wise). The value must be logical 0 for the start bit, and logical 1 for the stop bit. When the receiver detects no zero in the bit middle while scanning the start bit, it aborts synchronization. The stop bit with a logical 1 concludes correct synchronization. When a 0 bit occurs, this is interpreted as ERR-UART. The stop bit check can be disabled for testing purposes ("DIS-STOP-CONTROL = 1" in mode register 0). This setting may not be selected during normal operation since a Hamming distance of 4 would no longer be ensured. In addition, the receiver checks the parity bit and reports inequality with ERR-UART.

One requirement of the PROFIBUS protocol is that idle states are not permitted between telegram characters. The ASPC2 transmitter ensures that this specification is met. The ASPC2 receiver contains additional logic so that it can check external systems (e.g., software solutions) for compliance with this requirement. The receiver checks to determine whether start bit synchronization (not applicable to the last character of a telegram) immediately follows the stop bit. If this requirement is not met, it sets ERR-UART = 1. Parameterization of "DIS-START-CONTROL = 1" in mode register 0 disables this subsequent start bit check.

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The receiver is enabled by MS (ENAREC). After the receiver has completely received a character, it generates an RB-FULL. The MS then fetches the character and scans ERR-UART. When telegram characters are faulty, the MS rejects the entire telegram by disabling the receiver again.

6.5 FIFO

ASPC2 has only one FIFO which is set to the appropriate direction (i.e., receiving or sending direction) by the receive control bit. The 64/128-byte FIFO is used as intermediate storage for the telegram characters and thus for separation of the SER bus and the SYS bus. The FIFO consists of a dual-port RAM area with read and write pointers. It is located between MS and KS and is addressed by both. The MS controls the FIFO via an 8-bit port and the KS via a 16-bit port. Before one of the two enters the first character in the FIFO, it sets the FIFO to the appropriate direction (i.e., receive/send) and clears the contents of the FIFO (i.e., FIFO reset). The size of the FIFO can be set to 64 or 128 bytes.

6.5.1 Receive Mode

In receive mode, the MS transfers the telegram characters from the UART to the FIFO, and the KS transfers the telegram characters from FIFO to external memory. The MS writes the characters received from UART directly in the FIFO. When an entry causes a FIFO overrun, the MS terminates receiving, informs the KS of this, and generates the FIFO-error event interrupt. When the FIFO is a quarter full, it activates FIFO-QUARTER-FULL. The KS then takes over the SYS bus and transfers the complete contents of the FIFO to the memory.
When the 64-byte FIFO is used, the KS has a transmission time of 48 characters (approx. 40 µsec at 12 Mbaud) in which to take over the bus before a FIFO overrun occurs. When the 128-byte FIFO is used, the KS has a transmission time of 96 characters (approx. 84 µsec at 12 Mbaud) in which to take over the bus before a FIFO overrun occurs. This time defines the maximum external BUS-LOCK time. When a daisy chain is used, the sum of all BUS-LOCK times may not exceed the above stated time of 40/84 µsec at 12 Mbaud.
After the MS has entered the last character in the FIFO, FIFO-QUARTER-FULL is also activated so that the KS can transfer the rest of the data to the memory.
With 'Blocked-Mode = 1' and less than 58/122 bytes of data, the user data (layer 2) received by the master are not transferred to the external memory until they have be completely and correctly received (incl. FCS and ED). This parameterization is required for data consistency (e.g., the data are to be stored directly in the image memory). The SAP plausibility check is started for the slave as soon as the telegram header has been received correctly. ASPC2 does not transfer the user data (layer 2) to the external memory until it has received the data completely and correctly.

6.5.2 Send Mode

In send mode, the KS transfers the telegram characters from the external memory to the FIFO, and the MS transfers the telegram characters from the FIFO to the UART. The FIFO-QUARTER-EMPTY status line is active when the FIFO is at least a quarter empty. The KS then takes over the SYS bus and fills up the FIFO completely. As soon as a character has been entered in the FIFO, FIFO-BUSY becomes active. The MS then fetches the character from the FIFO and writes it in the UART. When the transmit buffer in the UART is free again, the MS fetches the next character from the FIFO, and so on. As soon as the MS can no longer guarantee sending without gaps since there are no more data in the FIFO (i.e., FIFO underrun), it terminates the sending procedure, informs the KS of this, and generates the FIFO-error event interrupt. The same times apply for taking over the SYS bus as in receive mode. A violation causes a FIFO underrun.

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7 Technical Data

This chapter contains only the most important parameters.

7.1 Maximum Limit Values

Parameter	Designation	Limits	Unit
DC supply voltage	VDD	-0.5 to 6.0	V
Input voltage	VI	-0.5 to VDD +0.5	V
Output voltage	VO	-0.5 to VDD + 0.5	V
DC input diode current	IIK	-20 to 20	mA
DC output diode current	IOK	-20 to 20	mA
Storage temperature	TST	-65 to 150	° C
Ambient temperature	TA	-40 to 85	° C
Chip temperature during operation	TJ	-40 to 125	° C
Power loss	Pv	Approx. 0.8	W

Table 6: Maximum limit values

7.2 Permissible Operational Values

Parameter	Designation	Min.	Max.	Unit
DC supply voltage (VSS= 0V)	VDD	4.5	5.5	V
Input voltage	VI	0	VDD	V
Output voltage	VO	0	VDD	V
Ambient temperature	TAI	-40	85	° C

Table 7: Permissible operational values

7.3 Guaranteed Operational Range for the Specified Parameters

Parameter		Min.	Max.	Unit
DC supply voltage (VSS=0V)		4 5	5.5	V
Ambient temperature		-40	85	° C

Table 8: Guaranteed operational range for the specific parameters

7.4 Specifications of the Output Drivers

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Signalname	Richtung	Treibertyp	Leistung	kap. Last
DB15..0	In/Out	Tristate	8mA	100pF
AB5..0	In/Out	Tristate	8mA	100pF
XBHE/XWRH	In/Out	Tristate	8mA	50pF
XRD	In/Out	Tristate	8mA	50pF
XWR/XWRL	In/Out	Tristate	8mA	50pF
AB19..6	Out	Tristate	8mA	100pF
RTS	Out	non–Trist.	8mA	50pF
TxD	Out	non–Trist.	8mA	50pF
XHTOK	Out	non–Trist.	8mA	50pF
DT/XR	Out	Tristate	4mA	50pF
X/INT–CI	Out	non–Trist.	4mA	50pF
X/INT–EVENT	Out	non–Trist.	4mA	50pF
HOLD	Out	Tristate	4mA	50pF
X/HOLDAOUT	Out	non–Trist.	8mA	50pF
XENBUF	Out	non–Trist.	4mA	50pF
XREQRDY	Out	non–Trist.	4mA	50pF
DIA9..0	Out	non–Trist.	4mA	50pF
XCLK2	Out	non–Trist.	4mA	50pF

Table 9: Specifications of the outputs

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7.5 DC Specification of the Pad Cells

Parameter		Bez.	MIN.	TYP.	MAX.	Einheit
Eingangsspannung 0–Pegel	CMOS	VILC			0.2VDD (5)	V
	TTL	VILT			0.8	V
Eingangsspannung 1–Pegel	CMOS	VIHC	0.7VDD (4)			V
	TTL	VIHT	2.0			V
pos. Schwelle Schmitt–Trigger	CMOS	VT+C			0.7VDD	V
neg. Schwelle Schmitt–Trigger	CMOS	VT–C	0.2VDD			V
Ausgangsspannung 0–Pegel		VOL			0.5 (1)	V
Ausgangsspannung 1–Pegel		VOH	VDD–0.8		(1)	V
Eingangsleckstrom 0–Pegel		IIL	–1			µA
Eingangsleckstrom 1–Pegel		IIH			1	µA
Ausgangsleckstrom 0–Pegel		IOZL	–10			µA
Ausgangsleckstrom 1–Pegel		IOZH			10	µA
Ausgangsstrom 0–Pegel 4mA–Zelle		IOL	4 (2)			mA
Ausgangsstrom 1–Pegel 4mA–Zelle		IOH	4 (3)			mA
Ausgangsstrom 0–Pegel 8mA–Zelle		IOL	8 (2)			mA
Ausgangsstrom 1–Pegel 8mA–Zelle		IOH	8 (3)			mA
Eingangskapazität		CIN	3,6		4,6	pF
Ausgangskapazität		COUT	4		5	pF
I/O–Kapazität		CIOUT	4		5	pF
Ausgangsstrom Pull–Up–Widerstand		IOPU	–5,5 µA <= IOPU <= 31,2 µA bei VAusgang = 0 V			µA
Ausgangsstrom Pull–Down–Widerstand		IOPD	80,7 µA <= IOPD <= 374 µA bei VAusgang = 5 V			µA

(1) belastet mit 4mA (8mA) bei 4mA (8mA) Pad–Zellen
(2) VOL = 0.5V
(3) VOH = VDD–0.8V
(4) maximal zulässiger AC Strom
(5) VDD = 4.5 ... 5.5V

Table 10: DC specifications of the pad cells

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7.6 Timing

7.6.1 SYS Bus Interface

No.	Parameter	Min.	Max.	Unit
1	Clock High Time	5,2*	15,6*	ns
2	Clock Low Time	5,2**	15,6**	ns
3	Clock Rise – Fall Time		5,2	ns
10	Address to XRD – Setup Time	27		ns
11	DT/XR Low to XRD – Setup Time	19		ns
12	XRD Active Width	(2 + 2n)T48 1)		ns
13	Address valid to Data valid		2(n–1)T48 + 83	ns
14	Data to XRD – Setup Time (8/16Bit–Mode)	27		ns
15	Data to XRD – Hold Time (8Bit–Mode) Hold Time (16Bit–Mode)	3 3		ns ns
16	DT/XR High to XRD – Hold Time	20		ns
17	Address to XRD – Hold Time	2T48		ns
18	XRD/XWR/XWRL – to XCLK2 – Setup Time	1T48		ns
19	Address to XWR/XWRL – Setup Time	23		ns
20	XWR/XWRL Active Width	(2 + 2n)T48 1)		ns
21	Data Valid to XWR/XWRL – Setup Time	(2+2n)T48–26		ns
22	Data to XWR/XWRL – Hold Time	2T48		ns
23	Address to XWR/XWRL – Hold Time	2T48		ns
	Quick–Access–Mode:			
25	Address to XRD – Setup Time	7		ns
26	DT/XR Low to XRD – Setup Time	0		ns
27	XRD Active Width	(1 + 2n)T48 1)		ns
28	Address valid to Data valid		2(n–1)T48 + 50	ns
29	Data to XRD – Setup Time (8/16Bit–Mode)	19		ns
30	DT/XR High to XRD – Hold Time	0		ns
31	Address to XWR/XWRL – Setup Time	7		ns
32	XWR/XWRL Active Width	(1 + 2n)T48 1)		ns
33	Data Valid to XWR/XWRL – Setup Time	(1+2n)T48–15		ns
35	XRDY to Clk48 – Setup Time	5		ns
36	XRDY to Clk48 – Hold Time	5		ns
37	XRDY Active Width	2T48+10		ns
38	XRDY – to XRD/XWR – Delay (kein zus. Waitstate)	2T48 2)	4T48 2)	ns
39	XRDY – to XRD/XWR – Delay (ein zus. Waitstate)	4T48 2)	6T48 2)	ns
40	Read–/Write–Cycle–Time (Quick–Access=0)	8T48 3)		ns
41	XRD; XWR/XWRL Inactive Delay zwischen aufein–anderfolgenden Wort–Zugriffen (Quick–Access=0)	4T48		ns
42	Read–/Write–Cycle–Time (Quick–Access=1)	6T48 3)		ns
43	XRD; XWR/XWRL Inactive Delay zwischen aufein–anderfolgenden Wort–Zugriffen (Quick–Access=1)	3T48		ns
44	XRD; XWR/XWRL Inactive Delay zwischen den bei–den aufeinanderfolgenden Zugriffen im 8Bit–Mode	3/4T48		ns

* Schwelle 3,5V
** Schwelle 1V

1) n = Anzahl der Waitstates
2) interne Waitstates sind schon abgelaufen
3) 1 internes Waitstate zu Grunde gelegt

Table 11: Specification of the processor bus interface

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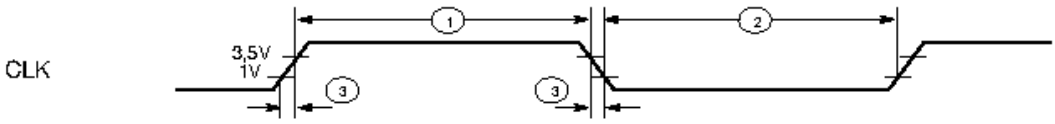

Figure. 8: Clock timing

7.6.2 Simple Access

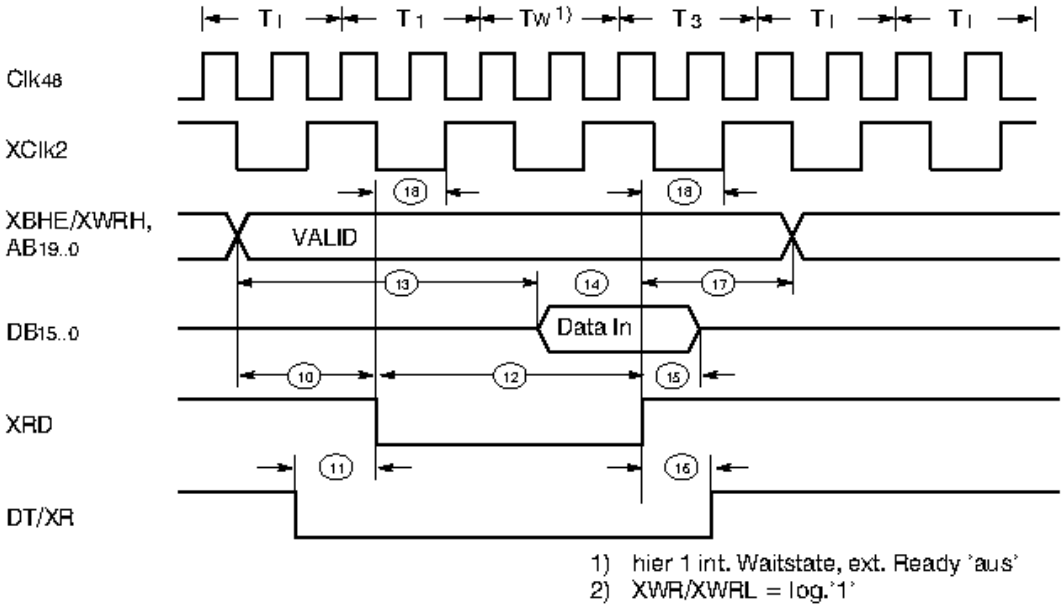

Figure 9: ASPC2 read timing

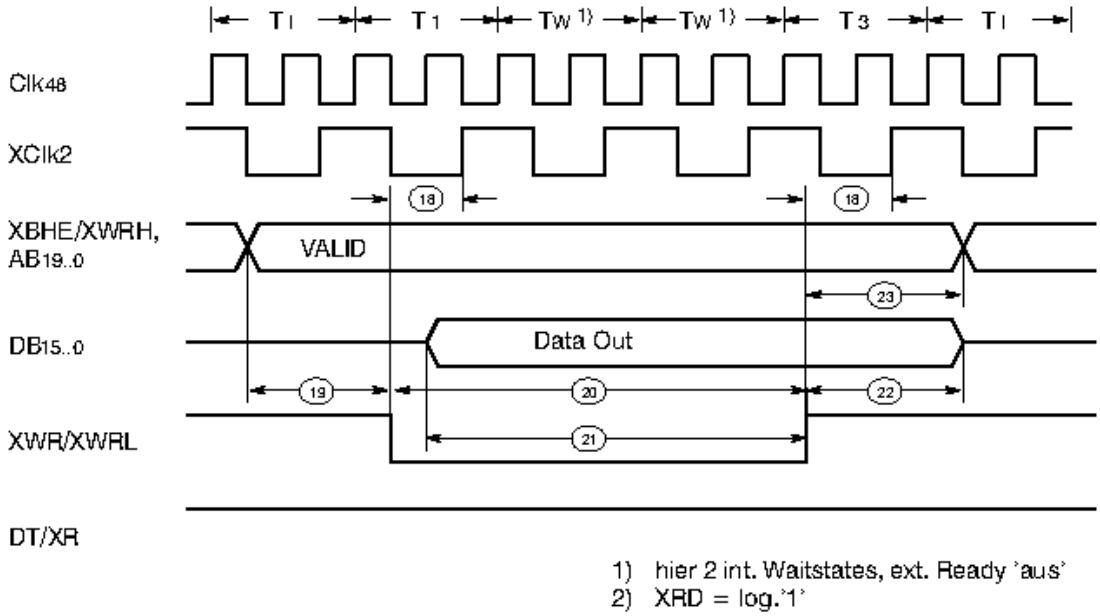

Figure 10: ASPC2 write timing

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7.6.3 Quick Access

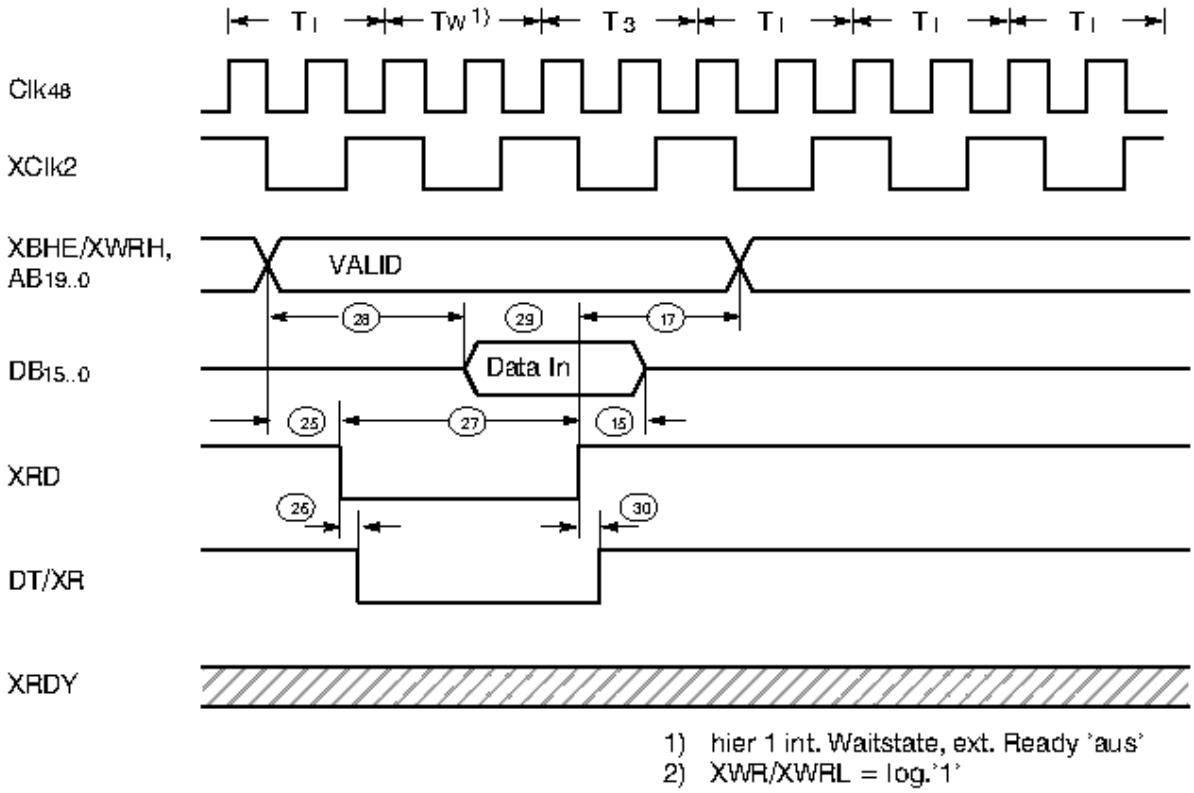

Figure 11: ASPC2 read timing

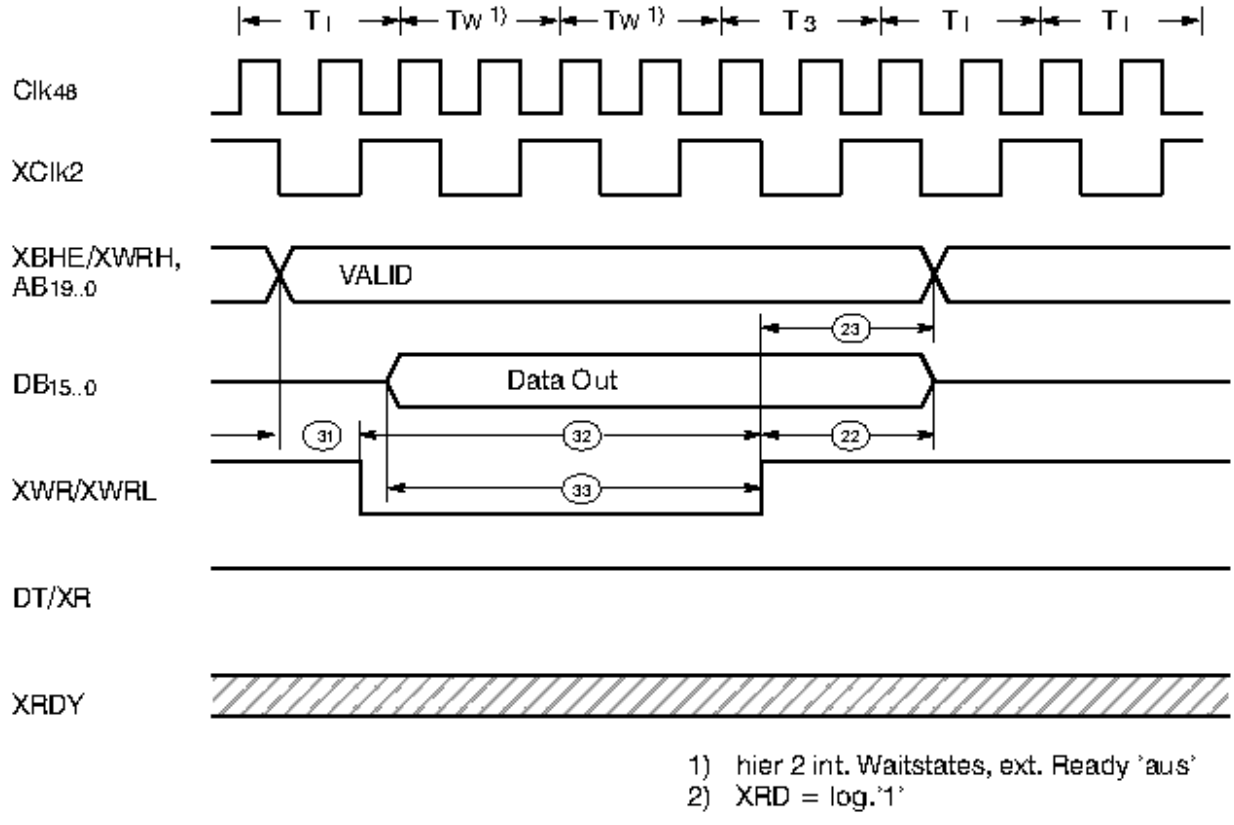

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Figure 12: ASPC2 write timing

7.6.4 Ready-Signal

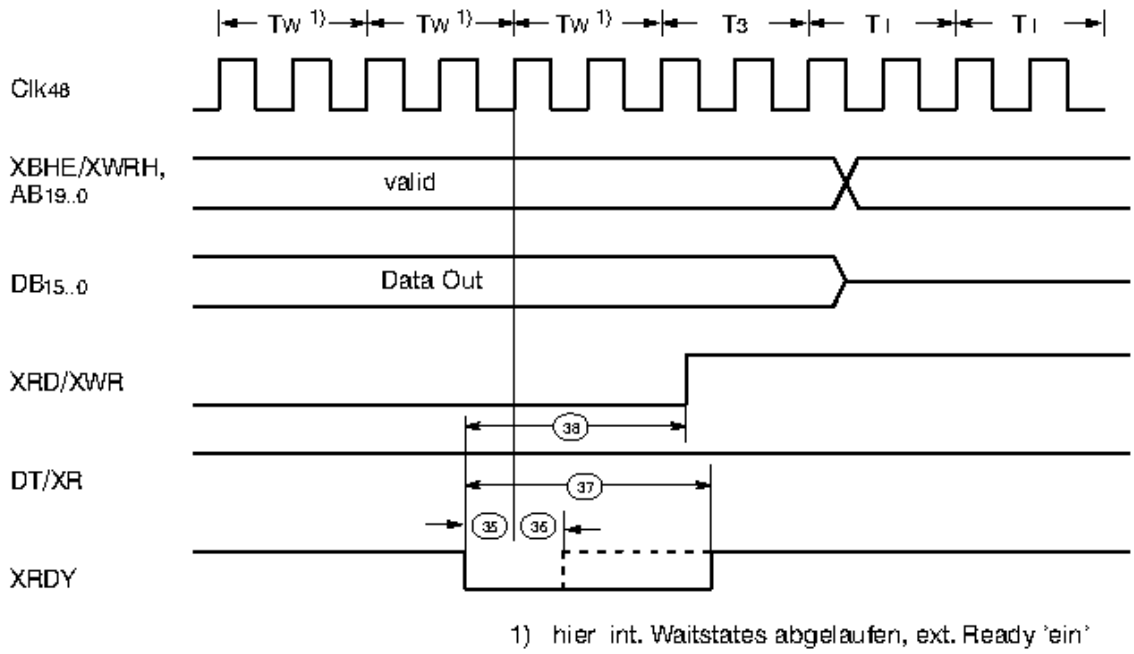

Figure 13: Ext. ready timing

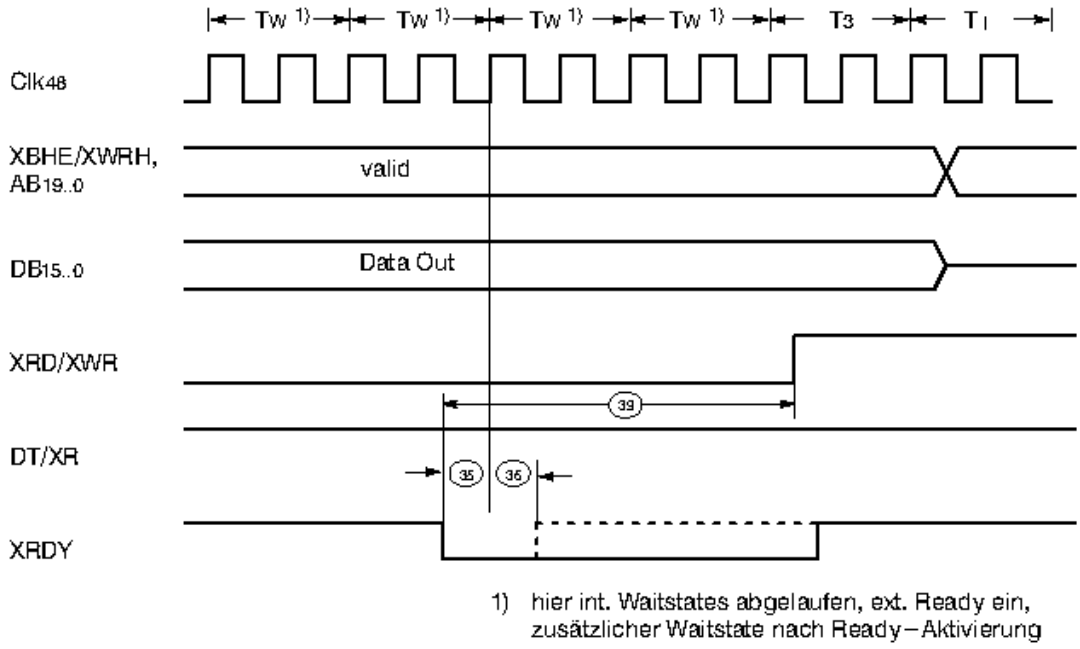

Figure 14: Ext. ready timing with wait state after ready activation

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7.6.5 Shared Memory

No.	Parameter	Min.	Max. 8Bit–Int.	Max. 16Bit–Int.	Unit
50	X/HOLDAIN to Command/Address Active Delay	2T48	6T48	6T48	ns
51	HOLD to Command/Address HiZ Delay	0			ns
52	X/HOLDAIN minimal Active Width	3T48			ns
53	min. Hold Inactive after X/HOLDAIN Inactive	2T48			ns
55	XREQ to XENBUF (BUSLOCK=0)	2T48	20T48	12T48	ns
	(BUSLOCK=1, ASPC–Lock=0)	2T48	20T48	12T48	ns
	(BUSLOCK=1, ASPC–Lock=1)	2T48	22,6 1)	11,3 1)	µs
56	XENBUF to XREQRDY (QREQRDY=0 in TQUI–Reg)	3T48			ns
	(QREQRDY=1 in TQUI–Reg)	1T48			ns
57 2)	XREQ to XENBUF/XREQRDY		1,5T48	1,5T48	ns
58	XREQ Inactive width	2T48 + 4			ns
60	RD/WRCONS to XRD/XWR	2T48			ns
61	XRD/XWR to RD/WRCONS	4T48			ns

1) FIFO komplett füllen (128 Bytes)
2) Spikes bei der steigenden Flanke von XREQ führen auch zu Spikes auf XENBUF und XREQRDY !
allgemein: Für jeden Speicherzugriff des ASPC 2 wurde 1 Waitstate zu Grunde gelegt.

Table 12: Specification of the hold/XREQ interface

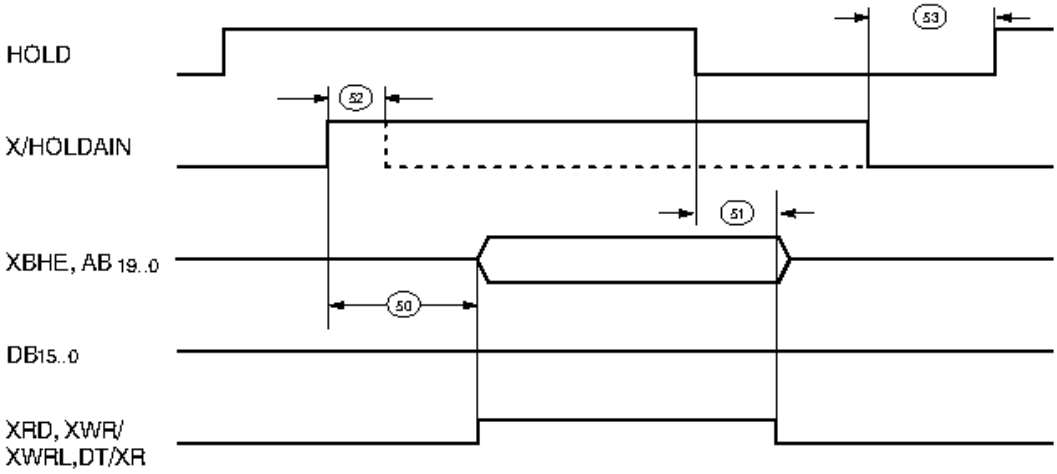

Figure 15: Hold timing

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7.6.6 Dual- Port Memory

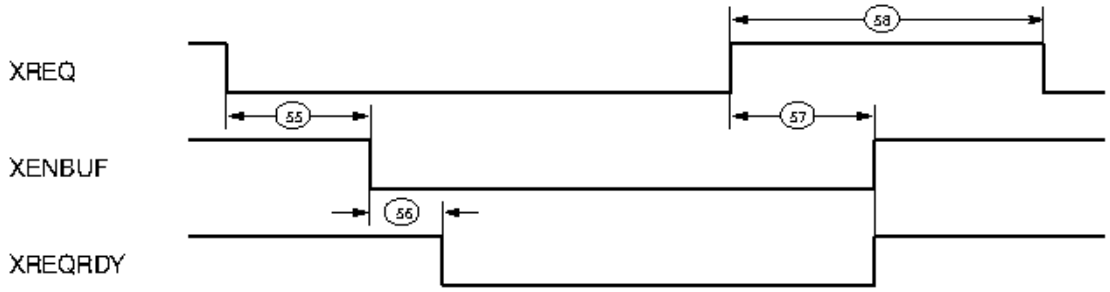

Figure 16: XREQ timing

7.6.7 Consistency Signals

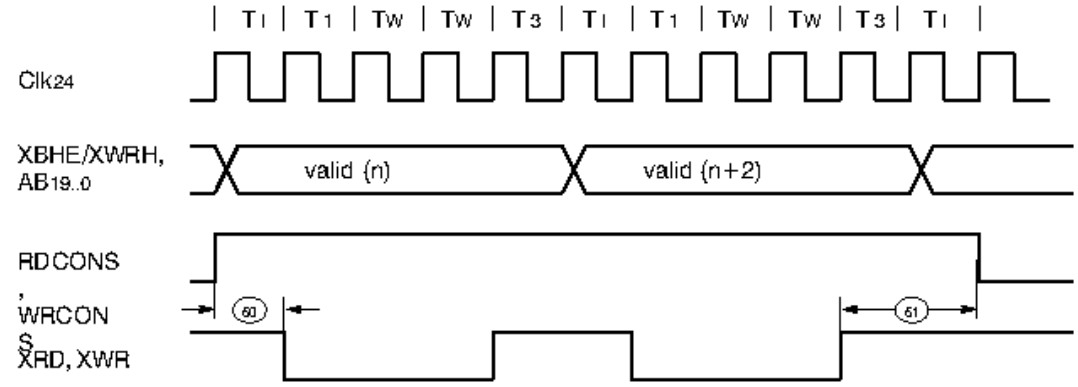

Figure 17: RDCONS-WRCONS timing

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7.6.8 Peripheral Mode

No.	Parameter	Min.	Max.	Unit
70	Address Required Valid to Read Data Valid Delay		20	ns
71	XCS – to Data Active Delay	3	18	ns
72	XRD – to Data Active Delay	3	18	ns
73	XRD Active width	$3T_{48}$ 1)		ns
74	Output Hold from Address change	2		ns
75	XRD – to Read Data HiZ	2	10	ns
76	XCS – to Read Data HiZ	2	10	ns
77	XRD Inactive Delay	$1T_{48}$		ns
		$9T_{48}$ 2)		ns
78	Address to XWR/XWRL – Setup Time	0		ns
79	XCS Low to XWR/XWRL – Setup Time	0		ns
80	XWR/XWRL Active width	$4T_{48}$		ns
81	Write Data Valid to XWR/XWRL – Setup Time	4		ns
82	Write Data Valid to XWR/XWRL – Hold Time	6		ns
83	Address to XWR/XWRL – Hold Time	0		ns
84	XCS – to XWR/XWRL – Hold Time	4		ns
85	XWR/XWRL Inactive Delay	$1T_{48} + 4$		ns
86	XWR/XWRL – to XRD – Inactive Delay	$1T_{48}$		ns
		$5T_{48}$ 3)		ns
		$9T_{48}$ 4)		ns
90	XREQ – to XCSASPC2 –		$1T_{48}$	ns
91	X/INT–Event Inactive Width (EOI–Timebase=0)	1000		ns
	(EOI–Timebase=1)	992	1025	µs
92	User–Timer–Clock–Period	10302,6	10334,6	µs

1) bestimmt durch den LAS–Zugriff
2) zwischen zwei Read–Zugriffen auf die LAS
3) bei Read auf IRR/IR nach Write auf IRR/IAR
   bei Read auf IR nach Write auf IMR
4) bei Read auf LAS nach Write 'LASREAD=1' (Mode–Reg. 1)

Table 13: Specification of the processor bus interface

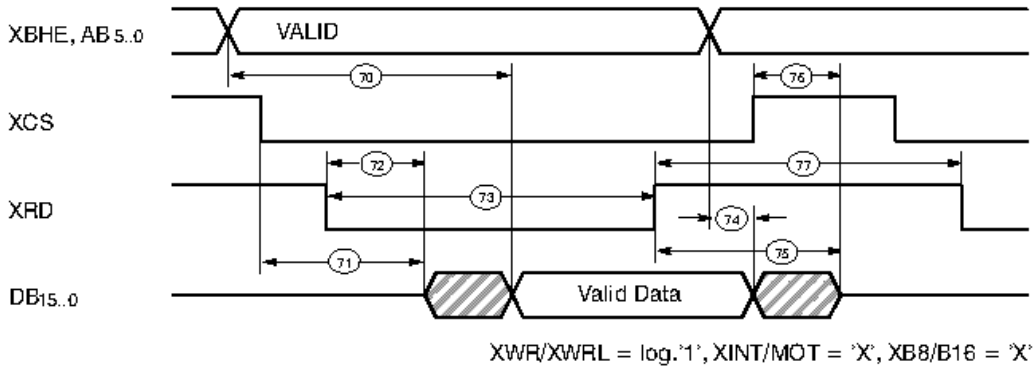

Figure 18: Shared memory, read-access to ASPC2

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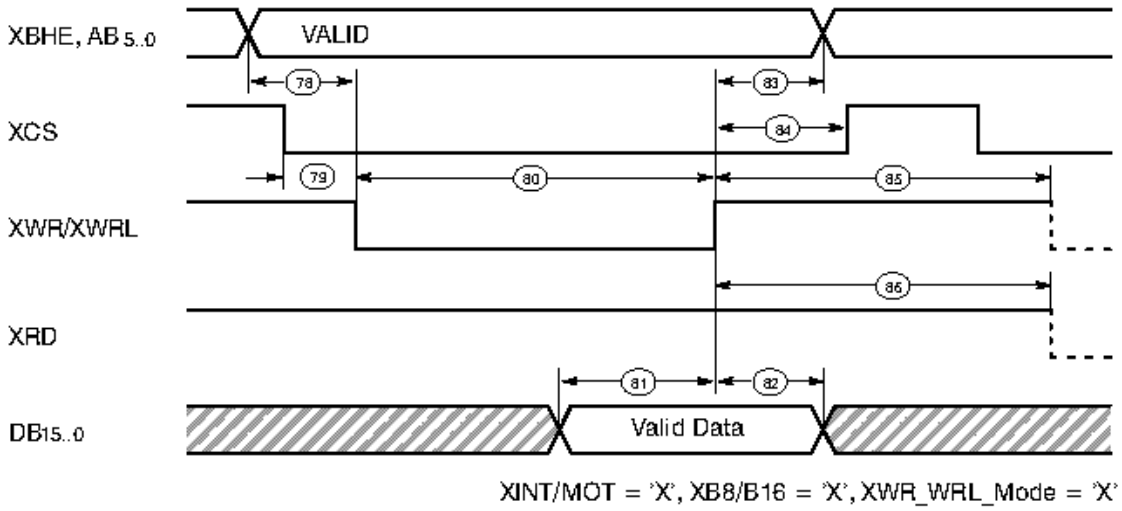

Figure 19: Shared memory, write-access to ASPC2

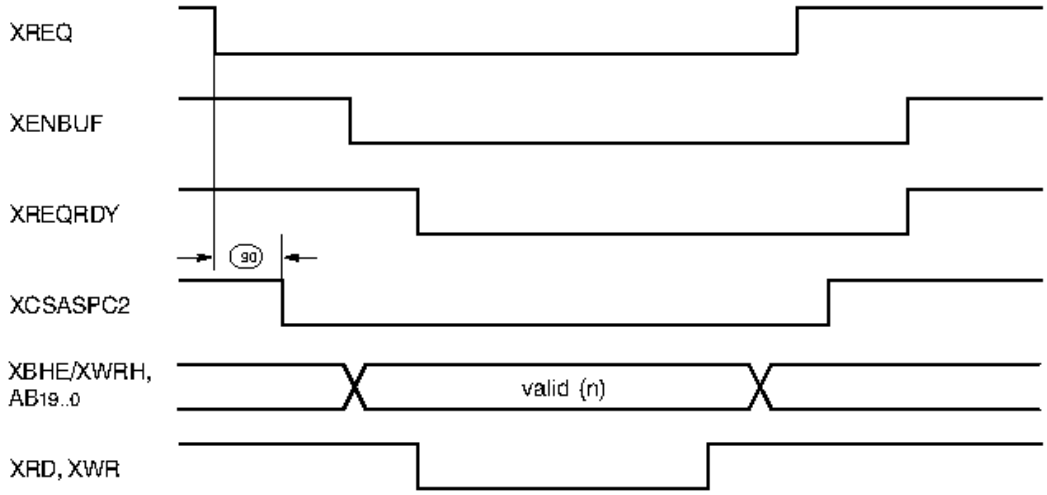

Figure 20: Dual-port memory: Processor access to ASPC2

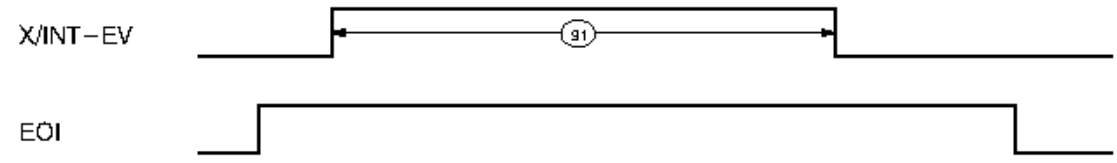

Figure 21: Interrupt EOI timing

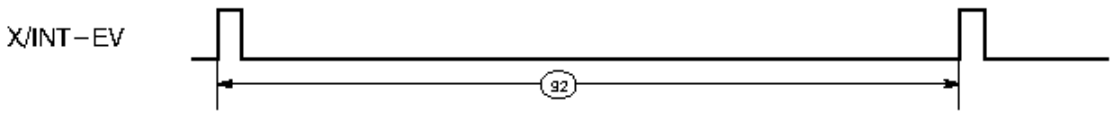

Figure 22: User timer clock period

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7.6.9 SER- Bus- Interface

No.	Parameter	Min.	Max.	Unit
95	RTS ⎓ to TxD Setup Time	5T48		ns
96	XCTS ⎓ to TxD Setup Time	3T48		ns
97	RTS ⎓ to TxD Hold Time	4T48		ns

Table 14: Specifications

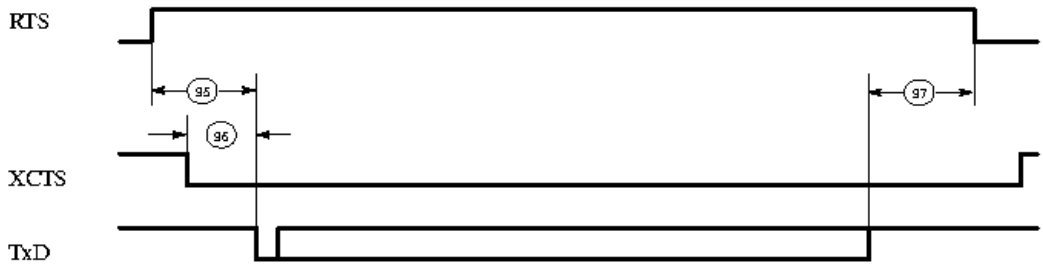

Figure 23: Transmit timing

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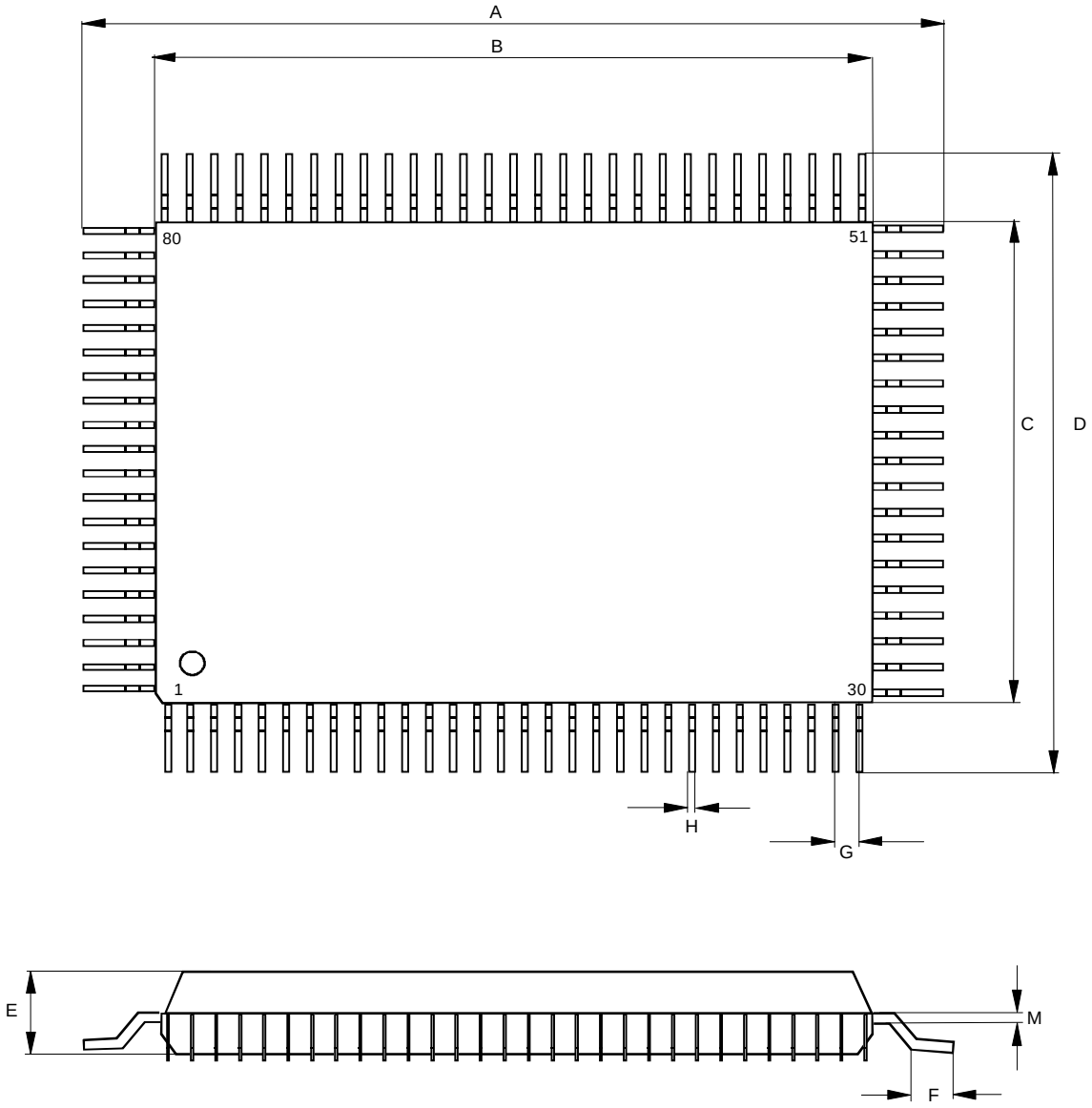
8 Housing (P-MQFP100)

P-MQFP100 Housing



A	23.20 + - 0.25	mm
B	20.00 + - 0.20	mm
C	14.00 + - 0.20	mm
D	17.20 + - 0.25	mm
E	2.70 + - 0.20	mm
F	0.88 + - 0.15	mm
G	0.65	mm
H	0.30 + - 0.08	mm
L	0.25	mm min
M	0.16	mm typ

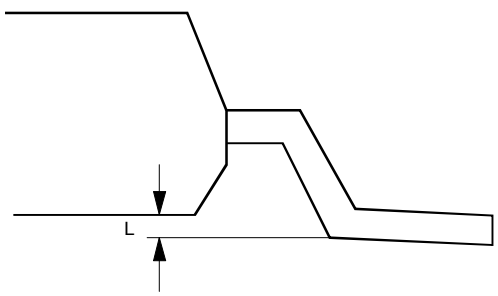


Figure 24: Physical housing

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9 Example

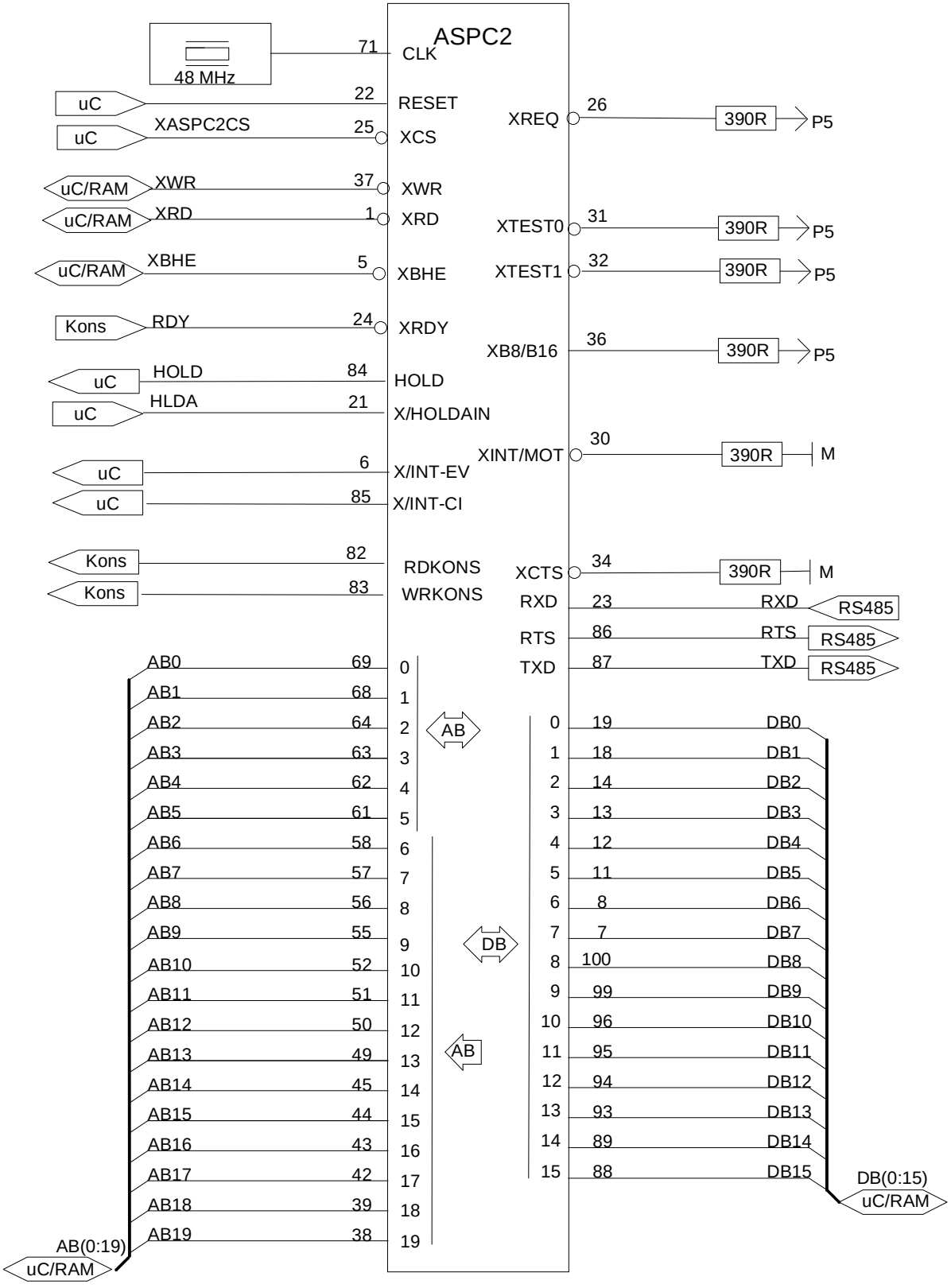

Figure 25: ASPC2 wiring

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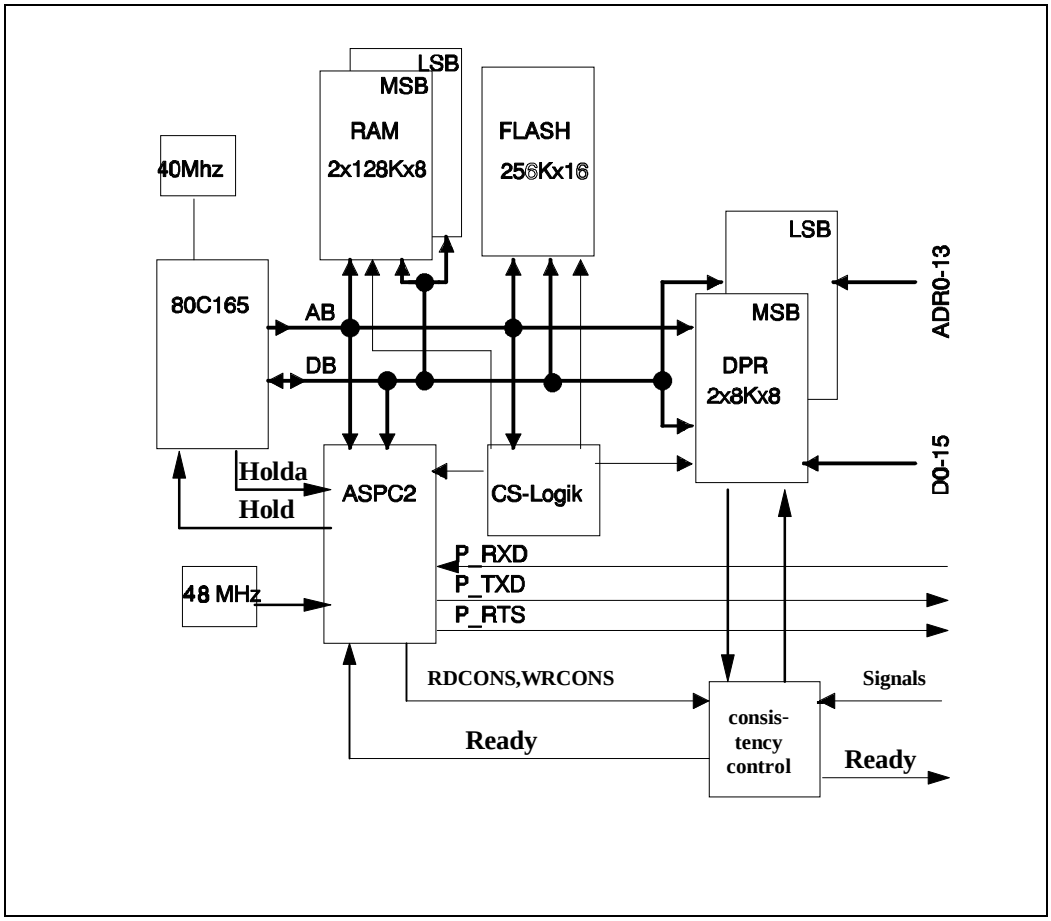

Figure 26: Sample overview

9.1 General

- ASPC2 and 80C165 are linked via ***Shared Memory Mode***.
- ASCP2 operates in **16-bit Intel Byte Ordering mode**.
- The **common** X/INT-EV interrupt line is used.
- Access to ASPC2 on the DPRAM is performed in **ready delay mode**.
- The consistency signals are applied to pins DIA0 and DIA1.
- Transfer to the FIFO is performed in **block mode**.

- 256-Kbyte RAM for system control, application and data blocks, and variables
- 512-Kbyte FLASH for binary program and parameter files (128 K for parameters)
- 16-Kbyte DPRAM for inputs, outputs and diagnoses of slaves

- The PROFIBUS signals can be circuited as shown in chapter.10.1.

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9.2 Consistency Control

Consistency control controls access to the DPRAM on both sides (i.e., the CPU and ASPC2 master side and the host side). Normally, the DPRAM briefly detains the other side with a ready-delay only when simultaneous access to the same address occurs.
When layer-2 data (i.e., inputs and outputs of the slaves up to the size of the 58/122-byte FIFO) are to be transferred consistently, the ASIC can activate the RDCONS and WRCONS signals on the master side by making entries in the job blocks for consistency control.
The host side requires appropriate signals so that consistency control can be set for the read or write-access.
When desired, the controller can use a hardware ready-disable to block the other side from access to entire memory areas.

9.3 Remarks

☞ All data which are accessed by ASPC2 must be located in a 1-MB area.

- Parameter data of COM ET200 V*.*
- DPRAM for inputs/outputs and diagnoses of the slaves
- Layer-2 data blocks for the transmission
- System control block and application blocks must also be located in a 64-Kbyte segment.

☞ The software uses the structure of the binary parameter file of COM ET200 for Windows.

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10 PROFIBUS Interface

10.1 Sample Circuiting for an RS 485 Interface

Data transmission is performed in RS 485 operating mode (i.e., RS 485 technology). Possible circuitry for PROFIBUS is shown below. The PROFIBUS interface is usually a 9-pin sub D socket.

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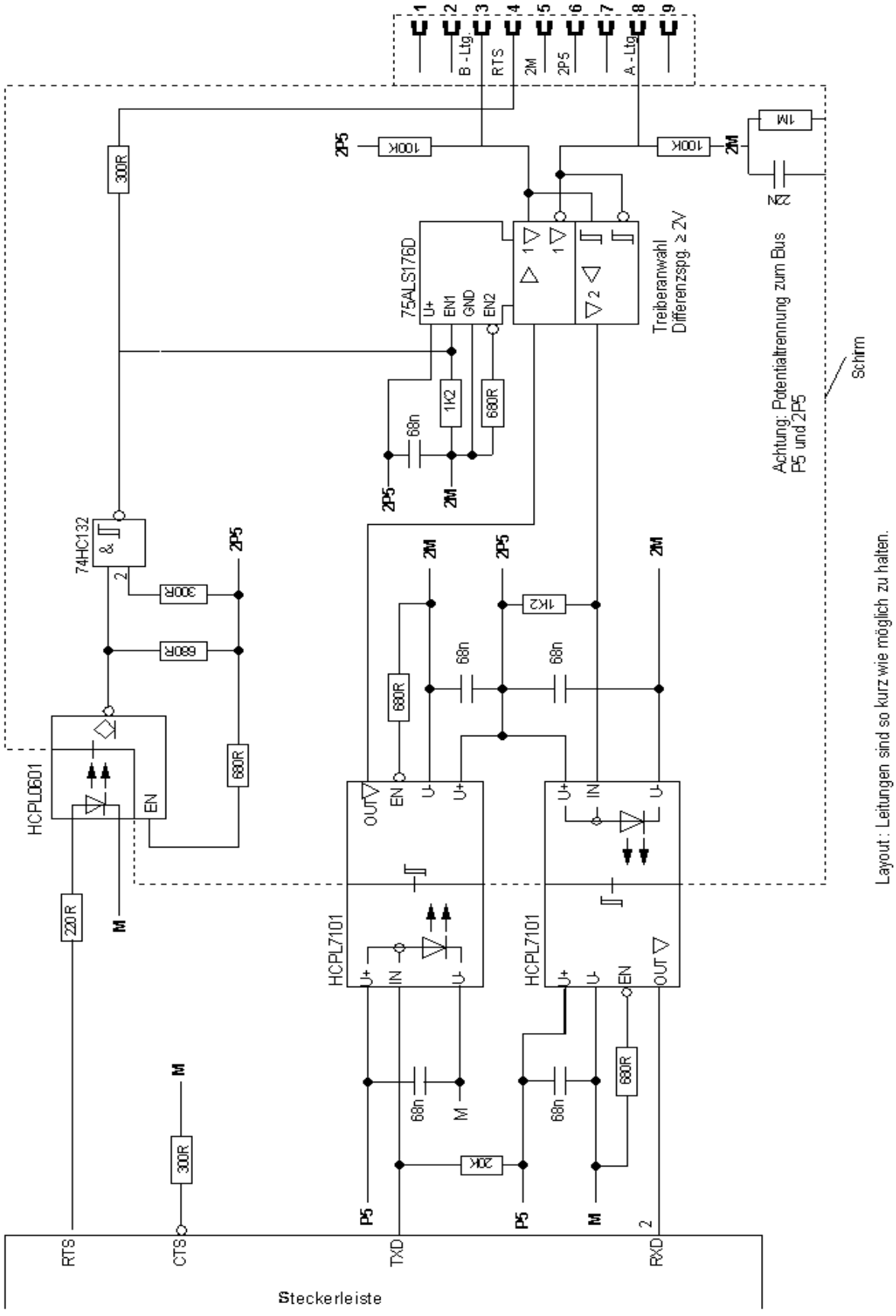

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10.2 Pin Allocation

Pin 1 - Not used
Pin 2 - Not used
Pin 3 - B-line
Pin 4 - Request to Send (RTS)
Pin 5 - Ground, 5 V **(M5)**
Pin 6 - Potential, 5 V **(floating, P5)**
Pin 7 - Not used
Pin 8 - A-line
Pin 9 - Not used

The line shield must be connected with the socket housing.
The unused pins are considered optional in EN 50 170. If used, they should conform to this standard.

CAUTION:
The line designations **A** and **B** on the socket correspond to the designations used in the RS 485 standard and not the pin designations used by driver ICs.
Keep the line from the driver to the socket as short as possible.

10.3 Plug Connectors

Siemens offers plug connectors to which terminating resistors can be added.

The use of special plug connectors is required when higher baud rates (i.e., 3 to 12 Mbaud) are used. These plug connectors compensate for line interference for all possible combinations of lines.

MLFB No.	Notes	Baud Rate:	Color of Connector Housing
6ES7 972 - 0BA00 - 0XA0	Without PG connection	Up to 1.5 Mbaud	Anthracite
6ES7 972 - 0BB00 - 0XA0	With PG connection	Up to 1.5 Mbaud	Anthracite
6ES7 972 - 0BA10 - 0XA0	Without PG connection	> 1.5 Mbaud	Anthracite
6ES7 972 - 0BB10 - 0XA0	With PG connection	> 1.5 Mbaud	Anthracite

10.4 Cable

Maximum cable and stub cable lengths must be observed as specified in the EN 50 170 standard, depending on the baud rates. If these values are not sufficient, repeaters can be used.

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11 Appendix

11.1 Address Reference

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Mr. Putschky

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Tel.: (0911) 750 - 2078
Fax: (0911) 750 - 2100
Mailbox: (0911) - 737972

Technical contact at the Interface Center in the USA

PROFIBUS Interface Center
3000 Bill Garland Road
Johnson City, TN 37605-1255

Fax : (423) - 461 - 2016
BBS:(423) - 461 - 2751

Your partners: Tim Black and Rainer Friess
Tel.: (423) - 461 - 2576

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11.2 List of Abbreviations

Most of the abbreviations used in these specifications are explained in the terminology data base. The list below mainly contains abbreviations which are not included in the data base.

APB	**Ap**plication **B**lock
ASPC2	**A**dvanced **S**iemens-**P**ROFIBUS-**C**ontroller **2**; ASIC
DP	**D**ecentral **P**eriphery
FLC	**F**ieldbus **L**ink **C**ontrol
HW	**H**ard**w**are
L2	**L**ayer **2** of the ISO/OSI-7 layer model
L4	**L**ayer **4** of the ISO/OSI-7 layer model
LSB	**L**east **S**ignificant **B**it
PROFIBUS	**Pro**cess **Fi**eld**bus**
SCB	**S**ystem **C**ontrol **B**lock; for the memory area required by ASPC2
SPC	**S**iemens **P**ROFIBUS **C**ontroller; ASIC
SPM	**S**iemens **P**ROFIBUS **M**ultiplexer; ASIC
USIF	**Us**er **I**nter**f**ace

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